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Review—Beyond the Highs and Lows: A Perspective on the Future of Dielectrics Research for Nanoelectronic Devices

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High-dielectric constant (high-*k*) gate oxides and low-dielectric constant (low-*k*) interlayer dielectrics (ILD) have dominated the nanoelectronic materials research scene over the past two decades, but they have recently reached a state of maturity and perhaps the limits of their scaling. Based on this, there is a need for a systematic review summarizing not only the historic research and achievements on high-*k* and low-*k* dielectrics, but also emerging device applications as well as an outlook of future challenges. We begin by first reviewing the factors that drove the emergence of low-*k* and high-*k* materials in nanoelectronics as ILD and gate dielectric materials, respectively, and the challenges and limits these materials ultimately approached in terms of permittivity scaling. We then illustrate that gate dielectric and ILD applications represent just a small fraction of the numerous dielectrics utilized in present day nanoelectronic products where permittivity scaling is now being increasingly demanded for materials such as dielectric spacers, trench isolation, and etch stopping layers. We conclude by examining the numerous new applications for dielectric materials that are emerging as the semiconductor industry transitions to novel patterning schemes, prepares for life post CMOS scaling, and explores ways to natively embed device functionality in the metal interconnect. For the former, we specifically examine the "colorful" requirements for the various enabling dielectric hardmask and spacer materials utilized in pitch division-multi-pattern processes and then discuss the role that selective area deposition of dielectrics and metals could play in reducing the complexity of such patterning processes. For the latter, we review the use of both high-*k* and low-*k* dielectrics in various metal-insulator-metal (MIM) structures as Fermi level de-pinning layers, tunnel diodes, and back-end-of-line (BEOL) compatible capacitive and resistive switching random access memory (ReRAM) elements. We further examine how dielectrics can hinder or aid new forms of computing such as quantum and neuromorphic in reaching their full potential. In conclusion, we find that while the field of dielectrics has a long history, it remains vibrant with numerous exciting new and old research vectors awaiting further exploration.
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For nearly the past two decades, high-dielectric constant (high-*k*) and low-dielectric constant (low-*k*) materials have dominated the nanoelectronic dielectric materials research scene as evidenced by the hundreds of articles published on these materials in journals of The Electrochemical Society (ECS). However, as shown in Figure 1, the number of publications for both class of materials peaked a little over a decade ago indicating a decline in research interest and funding, and also suggesting the achievement of a significant level of technological maturity. The latter is strongly supported by the numerous review articles and books that have now been published on high-*k*[1–7] and low-*k*[8–14] materials. With this in mind, one may ponder the future direction and vitality of dielectrics research in the semiconductor/nanoelectronics field. The goal of this article is to show that the well has not yet run dry and briefly overview the multitude of new and old research vectors that remain for dielectric researchers.

In this paper, we specifically seek to illustrate that high-*k* gate oxides and low-*k* interlay dielectrics (ILDs) represent just a small fraction of the numerous dielectric materials utilized in nanoelectronic products and that research into these "other" dielectrics remains a substantive and active field.[15–22] We further illustrate that, thanks to the numerous delays in extreme ultra-violet (EUV) lithography,[23,24] diverse new applications for dielectric materials have emerged as pitch-division multi-patterning technologies[25–27] have now come into widespread use. In addition, the numerous new devices being considered to extend and go beyond the end of the scaling roadmap for the currently dominant complementary metal oxide semiconductor (CMOS) device technology have created a bountiful new array of research opportunities for traditional and more complex dielectric materials.[28–31]

We begin by briefly reviewing the initial driving force for research into high-*k* and low-*k* materials, the current state-of-the-art and some of the remaining research challenges for these materials. We then attempt to explore the entirety of dielectric materials utilized in advanced nanoelectronic (logic) products with a particular focus on often ignored etch stopping, diffusion barrier, and passivation dielectrics and their more specialized requirements relative to high-*k* and low-*k* dielectrics.[21,22] Next, we transition to examining the various novel pitch division schemes being developed to cope with the delay of EUV lithography and the abundant new dielectric material applications these schemes create.[25–27] We specifically focus on the various new spacer and hard mask dielectrics that pitch division requires,[32–34] their colorful selectivity requirements,[32,35–37] and suggest future research needed to enable even more exotic patterning schemes based on selective area deposition methods.[32,38–40]

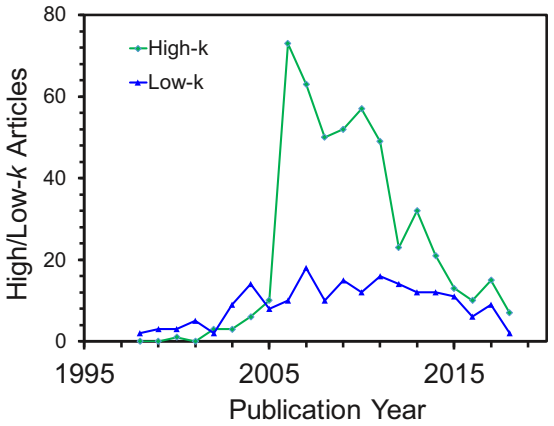

Figure 1. Number high-*k* and low-*k* dielectric articles published in journals of The Electrochemical Society (ECS) as a function of year.

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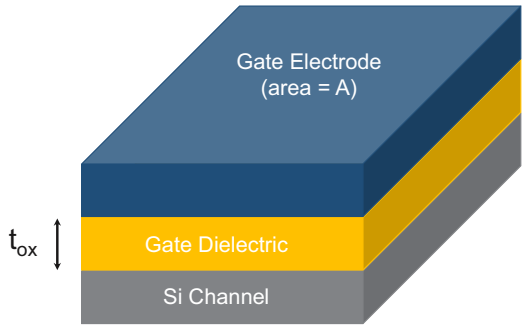

Figure 2. Schematic of a planar CMOS transistor as a parallel plate capacitor.

We then further examine how what was once old can become new again and specifically explore how both high-*k* and low-*k* dielectrics are being utilized to fill the needs of future beyond-CMOS devices. In particular, the application of high-*k* and low-*k* dielectrics in novel resistive switching,[41–43] negative capacitance,[44,45] ferro-electric,[46–48] magneto-electric,[49,50] and nano-electro-mechanical[51,52] devices will be surveyed. In addition, we also examine how these materials are also being utilized for gas sensors[53,54] and antimicrobial biological coating[55,56] applications and discuss the research needed to extend these materials into even more diverse applications.

Finally, we conclude by reviewing the unique obstacles that dielectric materials present for the realization of advanced cryogenic quantum computing architectures and the necessary associated research vectors to prevent dielectrics from becoming quantum computing's Achilles heel.[57–63] We do note that due to the authors' research backgrounds and affiliations, the presented perspective will be perhaps skewed toward nanoelectronic devices for logic and memory applications. However, it is hoped that this perspective will at least provide an illustrative (but not exhaustive) snapshot of the state of dielectrics research in the semiconductor/nanoelectronics field.

Why High-*k* and Low-*k*?

High-k.—High-*k* dielectrics first became of interest in CMOS devices to address the substantial and deleterious increases in gate leakage current the industry was facing as gate oxide thickness scaling approached only a few nanometers.[1,2] At these thicknesses, electrons could easily tunnel directly from the gate electrode, across the gate dielectric and into the channel, increasing off-state leakage and power consumption.[3] Since this tunneling leakage current increased exponentially with decreasing gate oxide thickness, there was a strong desire to find ways to replace SiO_2 with a physically thicker different material without degrading the gate oxide capacitance and thus sacrificing device performance.[4] As a CMOS field effect transistor (FET) is a capacitively operated device,[2] the source-drain current depends on the gate capacitance (C) which can be defined using the parallel-plate capacitor equation as:

$$C = k\varepsilon_0 A/t_{ox}, \quad [1]$$

where *k* is the relative dielectric constant of the gate dielectric material, ε_0 is the permittivity of free space, *A* is the area of the device, and t_{ox} is the thickness of the gate dielectric material (see Figure 2).

As can be seen from Eq. 1, an increase in capacitance can be achieved via replacing SiO_2 with a thicker material that has a proportionally higher dielectric constant (i.e. high-*k*). However, numerous technical requirements had to be fulfilled beyond just a high value of dielectric permittivity in order for a material to potentially replace SiO_2 as the gate dielectric. These included:[2,3]

1. A high enough *k* value to be re-used for several technology scaling cycles.
2. Thermodynamically stable when in direct contact with the Si channel region.
3. Kinetically stable with Si at processing temperatures of up to 1000°C for at least 5 seconds (i.e. remain amorphous).
4. Excellent insulating properties with Si interfacial band offsets of over 1 eV.
5. Form a good electrical interface with Si with low defect densities ($\leq 10^{10}/cm^2$).
6. Have few bulk electrically active defects – comparable to SiO_2 ($< 10^{17}/cm^3$).

Table I. Summary of amorphous high-*k* dielectrics initially considered to replace SiO_2 as the gate dielectric in Si CMOS devices with their respective values for dielectric constant (*k*), bandgap (E_g), and silicon valence band (ΔE_v) and conduction band (ΔE_c) offsets.

Dielectric	*k*	E_g(eV)	ΔE_v (eV)	ΔE_c (eV)
SiO_2	3.9[2]	9.0 ± 0.1[64]	4.5 ± 0.1[65]	4.0 ± 0.1[65]
Si_3N_4	7[2]	5.4 ± 0.1[66]	1.9 ± 0.1[66]	2.4 ± 0.1[66]
Al_2O_3	9[2]	7 ± 0.1[65]	3.8 ± 0.1[65]	2.1 ± 0.1[65]
AlN	8[7]	6 ± 0.1[77]	3.5 ± 0.3[78]	1.6 ± 0.3[78]
BeO	6.7[67]	8 ± 0.1[67]	4.6 ± 0.1[79]	2.6 ± 0.1[79]
Ta_2O_5	22[2]	4.7 ± 0.1[65]	3.2 ± 0.1[65]	0.3 ± 0.1[65]
$SrTiO_3$	2000[2]	3.3 ± 0.1[68]	2.1 ± 0.1[68]	0.0 ± 0.1[68]
TiO_2	80[2]	3.3 ± 0.1[69]	2.6 ± 0.1[69]	-0.2 ± 0.1[69]
ZrO_2	25[2]	5.5 ± 0.1[65]	3.2 ± 0.1[65]	1.2 ± 0.1[65]
HfO_2	25[2]	5.7 ± 0.1[70]	2.9 ± 0.1[80]	2.0 ± 0.1[80]
Y_2O_3	15[2]	6.0 ± 0.1[71]	3.5 ± 0.1[71]	1.3 ± 0.1[71]
Sc_2O_3	14[72]	5.6 ± 0.1[73]	3.7± 0.1[73]	3.0 ± 0.1[73]
La_2O_3	30[2]	6.4 ± 0.1[74]	2.3 ± 0.1[74]	3.0 ± 0.1[74]
$LaAlO_3$	30[2]	6.2 ± 0.1[75]	3.2 ± 0.1[75]	1.8 ± 0.1[75]

Table I provides a summary of some of the high-*k* oxides initially considered to replace SiO_2 as the gate dielectric along with their nominal values for dielectric constant (*k*), bandgap (E_g),[64–73] and valence band (ΔE_v) and conduction band (ΔE_c) offsets with Si.[64–80] For logic-based products, hafnium-based oxide dielectrics were found to be optimal for CMOS gate dielectrics.[81] The selection of HfO_2 was based primarily on its excellent performance against the previously mentioned selection requirements including a high *k* value ($\cong$ 25),[2] excellent thermal stability with Si,[82] manageable kinetic stability,[83] substantial band offsets with Si,[70] and good insulating electrical properties.[1–3]

Hafnium based high-*k* dielectrics were first introduced into commercially available 45 nm logic devices as announced by Intel Corporation in an IEEE International Electron Device Meetings article published in 2007.[84] This represents just a year offset between the peak in high-*k* research publications shown in Fig. 1 and actual implementation in a high volume manufactured (HVM) technology. While timeframes of 15–20 years are often quoted for the transition from discovery to deployment for new materials (i.e. the so called "valley of death"[85]), the short duration between peak research activity to implementation of high-*k* gate dielectrics in HVM provides an example of how new materials adoption can be accelerated through highly coordinated government and industry sponsored research.

For non-volatile flash memory applications, the charge trapping nature of the devices demands wide bandgap high-*k* dielectrics with substantial band offsets.[87] Al_2O_3 and other Al based oxide dielectrics with more modest *k* values of 7–30 have therefore been of primary interest in flash technology.[86,87] For volatile DRAM applications, the high-*k* requirements were similar to those for CMOS where a high-*k*, large bandgap, good electrical leakage, and thermodynamic and kinetic stability were also required.[86] For the later, a key difference though was the requirement for stability with a bottom metal electrode as opposed to Si in CMOS. In addition, a highly conformal high-*k* deposition process was also required to cover the high aspect ratio, three dimensional structures adopted.[88] This conformality requirement was readily achieved via atomic layer deposition (ALD) methods adopted during implementation of HfO_2 high-*k* gate dielectrics in CMOS.[89] However,

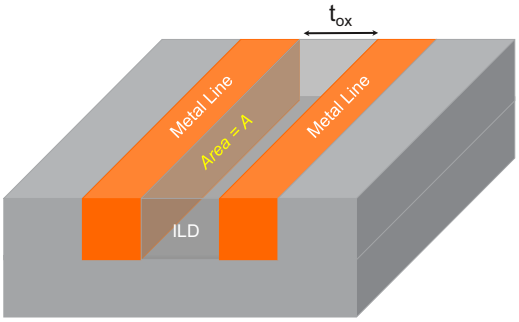

Figure 3. Schematic of a metal/ILD interconnect structure.

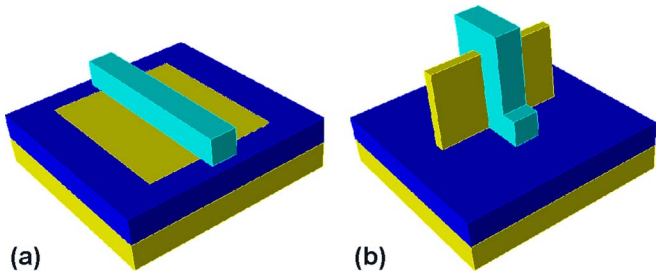

Figure 4. (a) Schematic of traditional 2D planar CMOS MOSFET transistor. (b) Schematic of 3D CMOS FINFET transistor. The light blue bar represents the gate electrode, the yellow region the Si channel, and the dark blue the local isolation.

a greater emphasis on capacitance scaling ultimately led to the selection of ZrO_2 over HfO_2 and other dielectrics for DRAM application.[90] ZrO_2 was primarily selected due to the greater ease to uniformly crystallize the initially amorphous ALD ZrO_2 film in down stream thermal processing to achieve the higher-k tetragonal phase (≅47). To mitigate the increased electrical leakage experienced upon crystallization while still preserving some of the higher-k, a multilayer $ZrO_2/Al_2O_3/ZrO_2$ (ZAZ) has been adopted by most DRAM manufacturers.[6,91]

For memory applications, high-k dielectrics had actually been of significant interest for more than a decade prior to CMOS, but initial efforts to implement high-k materials such as $SrTiO_3$ and $BaSrTiO_3$ were abandoned at the time due to various material and processing related difficulties.[86] This changed with the intense efforts to implement high-k gate dielectrics in CMOS and led to their renewed interest for both dynamic random access (DRAM) and flash memory applications. However, the requirements for high-k dielectrics in these applications had some significant differences relative to CMOS logic which lead to a divergence in the high-k materials selected.

Low-k.—In contrast to high-k materials, low-k dielectric materials emerged as an important class of research materials due to scaling issues in the metal interconnect brought about by the ever-decreasing gate delay times created by persistent transistor dimensional scaling.[9,11] Unlike transistors where the delay times decrease as the device size is scaled to smaller dimensions, the metal interconnect delay time increases with decreasing metal line-line separation.[92] The latter is a direct consequence of transistor density scaling as postulated by Moore's law.[93] For metal interconnects, the delay times are specifically associated with what are referred to as resistance-capacitance (RC) delays that are proportional to the product of the metal line resistance and the associated capacitance of the insulating interlayer dielectric (ILD) material.[92] The former led the semiconductor industry in the late 1990's to transition from using Al as the interconnect metal to Cu due to the significantly lower resistivity of Cu relative to Al.[94] However, the lack of compelling metals with resistivity lower than Cu led the industry to subsequently quickly focus on capacitance scaling to further reduce metal interconnect RC delays.

As a first approximation, the capacitance associated with the ILD can again be estimated using the classic parallel plate capacitor Eq. 1 where in this case, t_{ox} represents the metal line-line separation width (see Figure 3), A represents the metal line surface area, and k the dielectric constant of the ILD. As the metal line-line separation distance decreases due to combined transistor dimension and area scaling, t_{ox} will decrease increasing the capacitance and in turn interconnect RC delays. Therefore, one way to counteract the increased capacitance with shrinking metal line-line resistance is to adopt ILD materials with increasingly lower k values. To this end, the industry began implementing nearly two decades ago various forms of silicon dioxide (SiO_2) with reduced values of dielectric permittivity. The first so called low-k ILD was fluorine doped SiO_2 (SiOF) with a k of ∼ 3.7–3.9.[95] This material contained 3–5% fluorine and was primarily implemented in 0.18–0.13 micron technologies in the late 1990 time frame.[96,97]

Due to the need for continued capacitance scaling and the challenges of integrating SiO_2 with increased fluorine content for reduced k,[98,99] SiOF was soon replaced by so called carbon doped oxide (CDO) or organo-silicate (SiOCH) materials with k values of ∼ 3.0.[98] The first low-k SiOCH materials were implemented in the early 2000's for 90 nm technologies,[100–102] and quickly followed by higher organic content SiOCH materials with lower k values of 2.7–2.9 for 60–45 nm technologies.[11,102] Still lower k SiOCH materials were achieved and implemented in the late 2000's for ≤ 45 nm technologies through the introduction of nano-porosity as a second phase material with by definition a k value of 1.[102] This allowed SiOCH materials with a volume averaged $k < 2.5$ to be achieved.[10] Due to this widespread implementation and near continuous permittivity scaling, the term "low-k" is now virtually synonymous with SiOCH materials, despite SiOF representing the first low-k ILD.

The End of Permittivity Scaling?

With continued device scaling below 45 nm, one may have anticipated continued dielectric permittivity scaling for both high- and low-k materials and a continued exponential growth in published research on these materials. However, as Fig. 1 shows, research publications on high-k materials peaked in 2007 with a precipitous decline, while research in low-k materials remained relatively flat to 2015 before showing signs of decline. This disparate trend can be directly attributed to the different strategies adopted for transistor and metal interconnect scaling that, in turn, impacted dielectric permittivity scaling for both high- and low-k materials.

For CMOS applications, dielectric permittivity scaling has yet to progress significantly beyond the initial adoption of Hf based oxides which have been retained for successive technologies beyond 45 nm.[6,103,104] Some of the reasons for this are purely economical and a result of the semiconductor industry recouping part of the significant research expenditure needed to simultaneously identify, develop, implement and verify the reliability for the first material to replace SiO_2 as the gate dielectric material. In turn, reuse of Hf based gate dielectrics helped mitigate the risks associated with developing future subsequent technologies. This was particularly important for the recent technology nodes where the industry made the next significant pivot in CMOS transistor technology with the transition from traditional planar 2D transistors to newly developed FinFET 3D transistors (see Figure 4).[105] In this case, the continued use of Hf based oxides as the gate dielectric helped reduce the complexity of developing a new transistor technology while also avoiding the myriad reliability risks associated with both certifying a new gate dielectric material with a new transistor architecture. To date, Hf based high-k dielectrics are still in consideration for CMOS logic at 10 and 7 nm technologies.[104] As the CMOS scaling roadmap is currently heavily geared toward adopting new alternative channel materials (i.e. SiGe, Ge, GaAs, InAs, …) and/or new 1D nanowire transistors,[29,106] significant scaling of the gate dielectric permittivity in the near term seems unlikely.

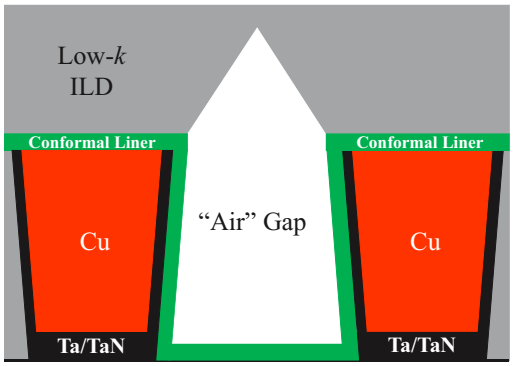

Figure 5. Schematic of "air"-gap metal interconnect structure.

In contrast, near continuous low-k dielectric permittivity scaling was pursued for nearly two decades after the first introduction of SiOF ILD in the late 1990's followed by the implementation of low-k SiOCH as previously discussed. This accounts for the consistent number of low-k research publications over the 2006–2015 time frame as shown in Fig. 1. However, the near continuous implementation of new low-k dielectrics with each new technology was not without significant and well documented challenges[107–111] that severely impacted the development of the associated metallization,[112–114] patterning,[115–119] and packaging[120–123] processes needed to fabricate a high yielding metal interconnect. By the mid 2010's, the challenges of implementing new low-k SiOCH ILDs with $k \leq 2.3$ had reached a breaking point relative to overall technology development goals for numerous reasons.[102]

On the technical side, the volume amount of porosity needed to achieve k values of < 2.3 went well beyond 30%[124–126] and the point at which pores switch from being primarily isolated (non-interacting) to highly interconnected.[127,128] The introduction of highly interconnected porosity dramatically increased the difficulty of developing new metallization and patterning technologies that retain the pristine as-deposited k value for the low-k ILD material.[129–131] At the same time, existing metallization and patterning technologies had reached their limitations and required the introduction of new materials[132] and techniques.[133,134] For metallization, the width of the metal lines for < 22 nm technologies had decreased to the point that the high resistivity Ta/TaN (TNT) Cu barrier material now represented close to 50% of the metal line and caused the metal line resistivity to increase exponentially.[135,136] This nullified the benefits of capacitance scaling by implementing increasingly difficult to integrate highly porous extreme low-k ILD materials.[102] Further, efforts to downscale the thickness of the TNT barrier[136–139] or adopt alternate metallization materials[140–145] to mitigate the resistivity impact were only exacerbated by the use of highly porous ILD materials. Similarly, continued delays in the availability of EUV lithography[146–148] forced the adoption of intricate pitch division/multi-patterning techniques[149,150] that multiplied the patterning induced damage and increase in k value for porous ILDs. To avoid the technical difficulties of simultaneously developing a new highly porous, extreme low-k ILD simultaneously with new metallization and patterning technologies, implementation of $k < 2.3$ ILDs has now been delayed or put on hold for multiple technologies.

The delay in adopting ILDs with $k < 2.3$ has also been mitigated to some extent by the recent development and implementation of so called "air-gap" interconnect structures.[151–153] In these technologies, various methods are utilized to either fully or partially replace the ILD in select locations by air which has a k of 1 (see Figure 5).[154–159] As k values < 1 cannot be achieved by definition, one can view this as the semiconductor industry reaching the ultimate limit in low-k dielectric permittivity scaling. However, air-gap technologies typically come with the added expense of additional material processing and patterning which presents a cost versus performance tradeoff.[160] The formation of air-gaps also introduces additional thermal-mechanical reliability concerns beyond those already typically associated with low-k dielectrics.[161–164] For these reasons, implementation of air-gap technologies in metal interconnects has been limited and only where there is substantial performance gain to be achieved.

What is Left for High-k and Low-k Dielectrics?

With the limits of low-k ILD permittivity scaling reached and high-k gate dielectric permittivity scaling on hold with new CMOS transistor designs and alternate channel materials taking priority, one may wonder what the future holds for low-k and high-k dielectric research. For high-k dielectrics, the good news is that the changes in consideration to support continued CMOS transistor scaling still create new opportunities for high-k dielectrics research beyond just permittivity scaling. Specifically, the growth of high-k dielectrics on alternate channel materials such as Ge, InAs, and InSb without Fermi level pinning and high interface defect levels is non-trivial.[165–171] Likewise, the nucleation and growth of high-k dielectrics on potential 2D channel materials and insulators such as graphene and MoS_2 is also non-trivial.[172–175]

Similarly, the insertion of air-gaps in metal interconnects while removing the low-k ILD from consideration at the targeted metal level, creates new complexities for the following low-k ILD used to pinch-off the air-gap structure shown in Figure 5.[154] The air-gap formation process also creates opportunities for other dielectric materials. Specifically, air-gap technology requires a dielectric that must conformally wrap around the bottom perimeter of the air-gap region and hermetically seal the exposed Cu metal surfaces prior to deposition of the pinch-off low-k ILD (see Fig. 5).[153] While the capacitance contribution of the low-k ILD has been removed and replaced by air with a k of 1, the air-gap liner still contributes to the capacitance and has a significantly higher k of > 4.[153] This is substantially higher than the k of the removed low-k ILD and mitigates some of the capacitance gained by forming the air-gap. In this regard, thickness scaling and finding lower k air-gap liner materials are important industry research topics.

It is also important to point out that while there is currently not a strong drive to implement new high-k gate oxide and low-k ILD materials with increasing or decreasing values of dielectric permittivity, these materials will remain and likely continue to be reused in multiple future single digit nanoelectronic technologies. Thus, there will be a continued need for improved understanding of the electrical,[176–181] thermal,[7,182–190] and mechanical[7,191–196] reliability of these materials as they are scaled to increasingly smaller dimensions. As such, research into such reliability issues will continue to be relevant and a constant focus until they are replaced with higher or lower dielectric permittivity materials.

Beyond high-k gate dielectrics and low-k ILDs, ultra-large scale integrated (ULSI) products contain numerous other dielectric materials that, while not previously receiving as much attention or publicity, are becoming increasingly more important in terms of achieving further dimensional scaling and performance gains.[18–21,197] In the following next section, we take a look at these frequently overlooked or forgotten about dielectrics and examine the unique permittivity scaling challenges they present and future research needed.

Overlooked Dielectrics and Low-k Everywhere!

As shown in Figure 6, numerous other dielectric materials exist at the transistor level that are utilized to help define and isolate the device.[197] These insulating layers represent parasitic capacitances to the device that are similar in nature to those previously described for the metal interconnect.[198–200] Reducing these device level parasitic capacitances has become increasingly important as gate and contact critical dimensions have been scaling slower than contacted gate pitch.[201] This means that parasitic fringe capacitances (such as the contact-to-gate and epi-to-gate, see Fig. 6a) are becoming increasingly more significant.[198] Similarly, parasitic capacitances associated with the shallow trench isolation (STI) are also becoming increasingly important (see Fig. 6b).

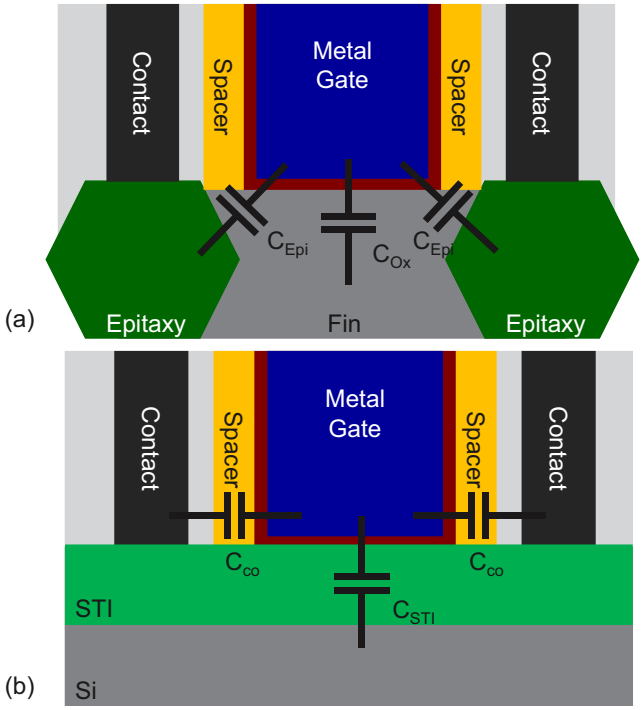

Figure 6. Schematic of CMOS FinFET illustrating various parasitic capacitances associated with the surrounding dielectrics.[198] (a) Cross section through contact over epi, (b) cross section through contact over isolation.

The primary path to reduce these parasitic capacitances is to reduce the dielectric constant of the spacer or STI dielectric or replace it all together with air-gaps such as those discussed previously in metal interconnect structures.[153,202] Traditionally, the spacer material has typically been SiN in composition with a nominally high-*k* of 7.[203,204] To reduce the capacitance associated with this high-*k* SiN, there have been recent reports of using alternate composition spacer materials such as SiBN,[205] SiBCN,[20] SiOC,[206] and SiO_2[19] with *k* values ranging from 5.5 to 4.0. However, spacer materials with still lower values of *k* are highly desired for future generation devices.[201]

Similarly, metal interconnect structures are composed of many additional dielectrics and metals beyond just the low-*k* ILD (see Figure 7). One of the more important dielectrics in this case is the Cu capping layer which serves multiple roles including passivating the top Cu surface to maximize electromigration performance, improving adhesion between Cu and the low-*k* ILD, preventing Cu diffusion into the low-*k* ILD to slow time dependent dielectric breakdown (TDDB), and acting as an etch stop (ES) for via or trench etching.[21] As with the

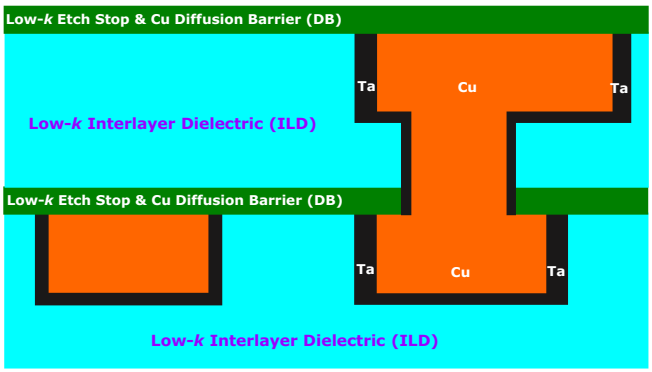

Figure 7. Schematic of low-*k*/Cu interconnect illustrating the presence of a low-*k* etch stop or Cu diffusion barrier dielectric.

low-*k* ILD, the ES contributes to the effective capacitance of the metal interconnect and the associated RC delays. There is therefore significant interest in methods to also reduce the dielectric constant of the ES. In the initial implementation of Cu damascene interconnects, the ES was PECVD SiNH with a modestly high-*k* of approximately 7.[92,207] Since then, lower-*k* SiCN, SiOC, and SiC films with *k* as low as 4 have been demonstrated and adopted in the industry.[208–214] Recent experiments have also shown that high carbon content SiCH films with *k* as low as 3.2 may be suitable as next generation ES/DB materials.[215–217] However, there are scaling limits in *k* due to the need to maintain a dense enough material that can still function as a Cu diffusion barrier (DB) material as well as ES.[218] As for the transistor, boron-based materials such as BNH[219–222] and BCH[223,224] have also shown some promise as potential lower-*k* ES/DB candidates. As we will discuss later, additional etch considerations created by the more complex patterning schemes recently adopted have led to the exploration of a still wider range of materials as candidate ES/DB materials.

Spacers and Hard Masks – The Disappearing Dielectrics

As alluded to previously, the numerous delays in the availability/manufacturability of EUV lithography[23,24] has forced the industry to adopt more complex pitch division/multi-patterning photolithography methods to continue traditional Moore's law driven dimensional down-scaling.[25–27] As we will describe next, these new patterning schemes created numerous new applications and challenges for dielectric materials within the semiconductor industry.[149,150] To illustrate the changes adopted in pitch division/multi-patterning methods and how they create new opportunities for dielectric materials, we briefly examine the patterning methods typically employed to pattern low-*k*/Cu interconnect layers for technologies just before pitch division/multi-patterning methods were typically adopted. We then present the methods commonly utilized to pattern similar layers at reduced dimensions using pitch division methods with an emphasis on the new dielectric materials employed.

At the 45 nm logic node, the most common method for patterning the tightest pitch low-*k*/Cu interconnect layers utilized traditional single exposure 193 nm dry optical lithography and what was referred to as a metal hard mask approach.[225,226] This approach was adopted primarily to reduce patterning induced degradation of the low-*k* ILD dielectric constant and enable etching of high aspect ratio features.[227,228] The success of the approach was based primarily on the ability to selectively etch the overlying metal hard mask relative to the low-*k* ILD[227] and the metal hard mask to shield and protect the underlying low-*k* ILD from the various subsequent damaging plasmas used to perform the pattern transfer etch and cleans (see Fig. 10).[228] Titanium nitride (TiN) was commonly selected for this application due to its acceptable transparency,[229] high etch selectivity relative to other dielectric hard mask materials such as C:H and SiC:H,[230] and the ability to be removed in subsequent post etch wet cleans.[226,227]

However, traditional single pass dry optical lithography methods utilizing 193 nm wavelengths became incapable of printing the finer dimensions needed for < 45 nm technologies and the lack of EUV readiness forced the transition to both immersion lithography[231–234] and pitch division/double patterning methods.[25–27] At a high level, all three patterning methods can be understood through the Rayleigh equation which states that the minimum resolution (*R*) of an optical lithography system can be defined as:

$$R = k_1 \lambda / NA, \quad [2]$$

where k_1 is a process dependent constant, λ is the wavelength of the optical imaging system, and *NA* is the numerical aperture of the projection lens. With EUV, the resolution is improved directly by moving to shorter wavelengths of light.[24] However, the resolution for an immersion lithography process is improved instead by increasing *NA* via inserting water with a higher refractive index than air in between the lens and the wafer.[234] In contrast to both EUV and immersion lithography, pitch division methods take advantage of the fact that *R* is not simply the dimension of the desired printed feature but the pitch:[235] the

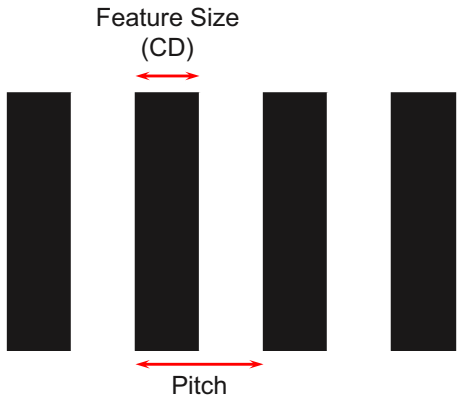

Figure 8. Schematic illustrating the relationship between feature size, critical dimension (CD), and pitch in optical lithography.

feature size (or critical dimension (CD) plus the space-width between features (see Figure 8).

In traditional optical lithography, the CD/space ratio has been typically tuned to 1:1 where the CD is just half the pitch width. However, other ratios can be adopted. In pitch division processes, the optical lithography process is adjusted to achieve the desired CD, but since the pitch is fixed, the space between features increases. To obtain the desired feature density, half the desired pattern is printed and then the other half of the pattern is printed shifted by half the pitch relative to the other in a second litho-etch pass (see Figure 9). In order to produce fully functional metal interconnect structures, such litho-etch-litho-etch (LELE) patterning must be combined with additional litho-etch "cut" steps to convert the printed lines and spaces into the desired metal line layout.[236,237] From a dielectric perspective though, this form of pitch division patterning has led to the implementation of additional dielectric hard masking materials such as a-C:H, a-Si:H, a-SiN:H, a-SiOC:H and SiO_2 to enable the various different additional litho-etch steps and enable reflectivity control during optical lithography (see Fig. 10).[149,238–243]

While LELE double patterning methods are technically achievable, they require multiple passes through slow and expensive optical patterning steps and have challenges associated with layer-to-layer alignment and registration between the first and second litho-etch steps that can lead to significant edge placement error (EPE) issues.[31] To help reduce processing costs and EPE, self-aligned multi-patterning (SAMP) approaches have been developed as an alternative.[149,150] In this approach, standard optical lithography and patterning methods are utilized to print a template pattern on the wafer that is sometimes referred to as the "core" or "mandrel".[244] A thin and conformal dielectric

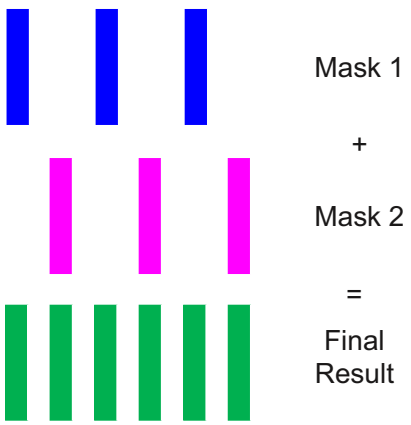

Figure 9. Schematic illustrating pitch doubling/double patterning.

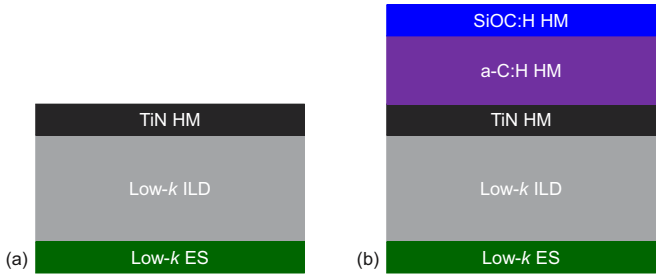

Figure 10. Schematic illustrating generic film stacks utilized for patterning low-*k* ILD (a) using standard 193 nm dry optical lithography, (b) 193 nm immersion optical lithography and pitch division – multi patterning.[26]

film is then deposited over the pre-patterned features and etched back by dry plasma to form what is referred to as a "spacer" on the core sidewalls (see Figures 11a–11c).[149,150] To form a self-aligned pitch doubled pattern, the core material is then selectively removed to leave only the standing spacer material, and the spacers are then utilized as a hard mask to transfer the formed features directly into the target material (see Figs. 11d–11f).

Although SAMP approaches alleviate some EPE challenges, they do come with additional limitations related to design rule and layout restrictions.[245] They are also limited in some regards by various attributes of the spacer material. Specifically, any thickness variation or surface roughness in the spacer material can directly impact, respectively, the CD and line edge/width roughness (LER/LWR) of the final formed feature.[149,150] Similarly, any vertical slope/taper or asymmetry (geometrical or material properties) in the formed spacer can directly affect the CD and profile of the final feature.[246] Further, the mechanical properties and intrinsic stresses in the spacer and associated hard mask materials must be carefully considered in order to prevent pattern collapse and line wiggling issues.[118,119,247–249]

The spacer material and deposition process must also be compatible with the pitch division process and hard masking materials utilized to form the initial template. In cases where a high temperature deposited a-C:H film is chosen as the template material, a similarly high temperature CVD or PECVD oxide/nitride material may be suitable.[149] However, in cases where it is desired to use photoresist as the template core, a much lower temperature ALD or PEALD SiO_2 spacer deposition process may be preferred.[150] Aside from temperature constraints, dielectric deposition directly on photoresist also requires careful consideration to sources of amines which may poison the photoresist and complicate removal later.[250–252] Finally, the dielectric spacer material must not only have high etch selectivity relative to the photoresist and other hard mask materials, but also must have the ability to be easily removed later using wet or dry methods. While all these many considerations are clearly aggravating points for lithographers and patterning specialists, these clearly create new and exciting research opportunities for dielectric researchers!

It should also be noted that even with the eventual readiness of EUV lithography, pitch division/multi-patterning methods will still likely be needed in combination with EUV to print < 10 nm features.[246,253] In the absence of EUV, triple and quadruple patterning/pitch quartering methods will clearly be needed to reach < 20 nm CDs.[254] As shown in Figure 12, such schemes will require multiple different hard mask, anti-reflection, spacer, and photoresist materials to be achieved.[255,256] While there are many considerations, the success of schemes such as the one illustrated in Fig. 12 is largely dependent on identifying a unique set of materials with sufficiently different dry etch properties that they can be selectively etched or left behind as needed to form the desired final pattern. The identification and selection of such unique combinations of materials and etches is a non-trivial problem and creates yet another area of opportunity for dielectric researchers to be discussed next.

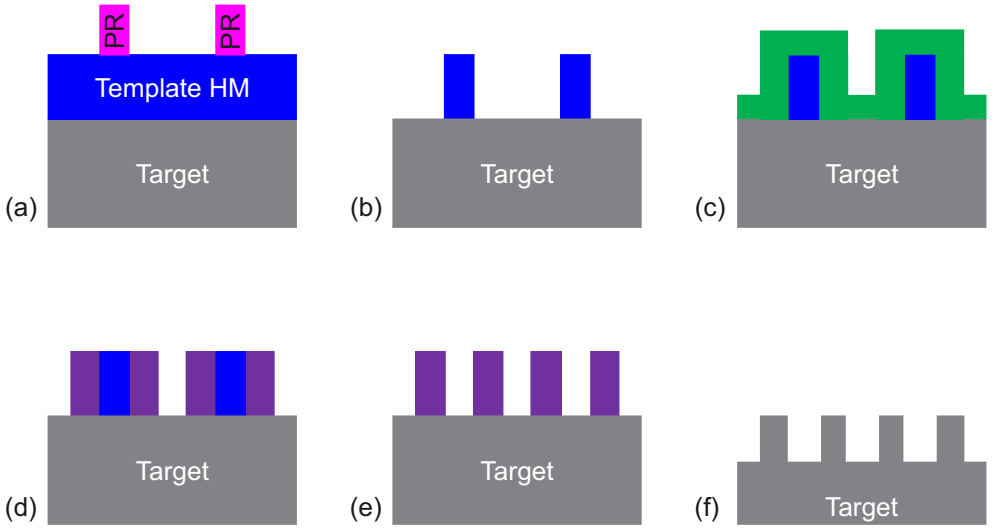

Figure 11. Generic flow illustrating self-aligned multi-pattern (SAMP). (a) Starting film stack is target material to which final pattern is to be transferred, template hard mask (HM) material, and photoresist (PR) patterned using standard dry or immersion 193 nm optical lithography, (b) dry etch transfer of PR pattern into template HM and formation of mandrel, (c) deposition of conformal film over mandrel, (d) partial etch and planarization of conformal film to form spacer, (e) selective removal of the mandrel to form pitch double spacers, and (f) final dry etch transfer of spacer pattern into target material.[149]

Color Technology and The Four-Color Problem

As depicted in Figs. 10–12, the easiest way to view the etch selectivity requirements for pitch division multi-pattern processes is to consider each material with distinct etch properties as having a different "color".[32] This in turn allows what is referred to as the four-color theorem to be invoked[36] which comes from map theory and states that only four colors are needed to color a map such that no two bordering countries will have the same color.[257] In this regard, a wafer being patterned by pitch division/multi-pattern methods may be considered as a checkerboard array of different materials that are exposed simultaneously during any given plasma etch pattern transfer step (see Figure 13).[35] Viewed this way, application of the four-color theorem suggests that only four complementary materials and etches with perfect selectivity relative to one another should be needed to achieve any multi-pattern pitch division process. Unfortunately, such color technology of materials does not fully exist, and the current set of materials currently employed represent at best two – three distinct colors.[32] Thus, there is a significant research need to identify suitable third and/or fourth color materials to expand the color palette for multi-pattern processes.

In this regard, traditional high-*k* oxide[33,34,258–260] and nitride[261–263] dielectrics have re-emerged as potential hard masking and spacer materials in multi-pattern processing. This is primarily a result of their high optical transparency and strong resistance to fluorine based dry etches.[37,264] Similarly, boron-based dielectrics have also gained significant interest as alternative or complementary hard masking materials[265,266] due to their significant dry etch rates in fluorine-based chemistries,[37,219,267] low wet etch rates in dilute HF,[223,268] and tunable bi-axial film stress[37] and mechanical properties.[264,269] The high resistance of high-*k* oxides and nitrides to fluorinated plasma chemistries

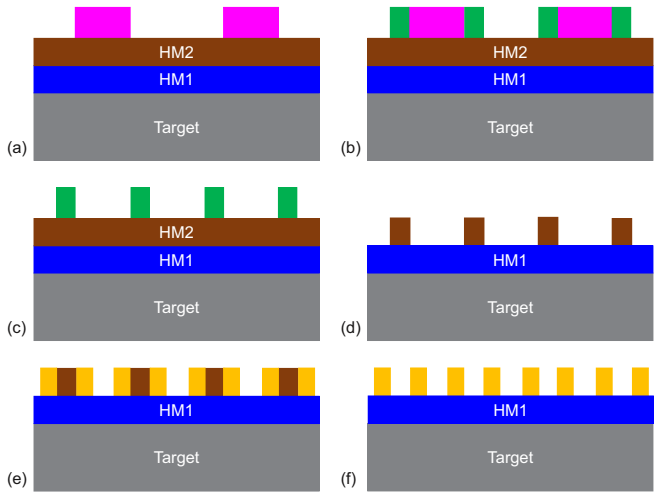

Figure 12. Generic flow illustrating self-aligned pitch quartering scheme. (a) Starting film stack is target material to which final pattern is to be transferred, template hard mask material number 1 (HM1), template hard mask material number 2 (HM2), and photoresist patterned using standard dry or immersion 193 nm optical lithography, (b) deposition of conformal spacer material and partial etch and planarization to form sidewall spacer, (c) selective removal of the mandrel to form pitch double spacers, (d) dry etch transfer of spacer patter pattern into HM1, (e) deposition of second conformal spacer material and partial etch and planarization to form sidewall spacer, (f) selective removal of the HM1 mandrel to form pitch quartered spacers.[255,256]

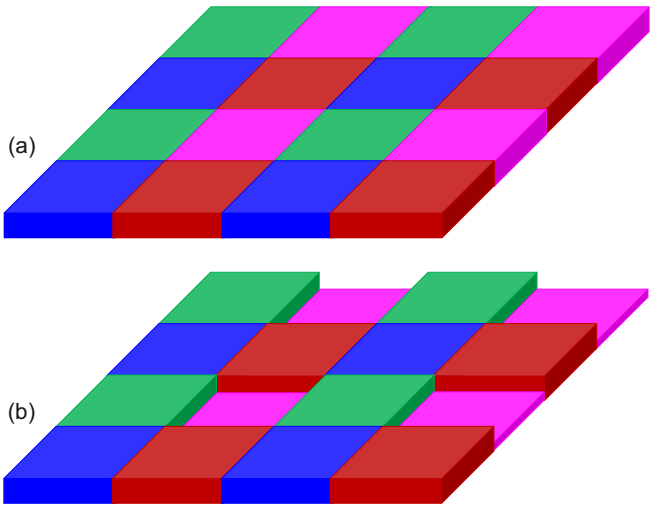

Figure 13. (a) Schematic illustration of a four-color patterning scheme for a pitch division multi-pattern process scheme where, (b) one color/material may be etched with perfect selectivity relative to the other three colors/materials.[35]

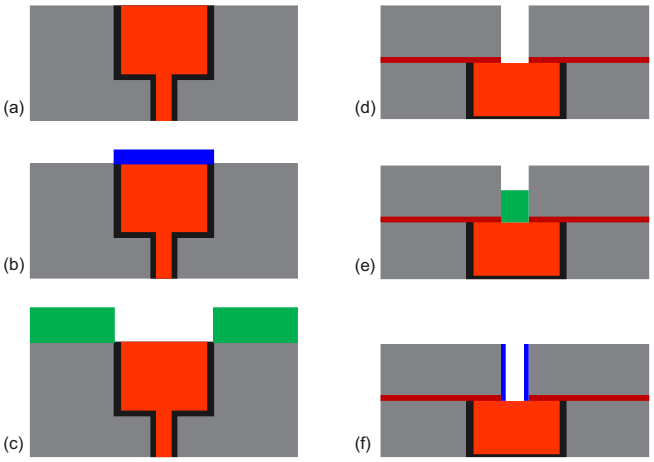

Figure 14. Schematic of desired selective metal or dielectric deposition. (a) Planarized dielectric with inlaid metal line, (b) selective growth/deposition of metal on metal line, (c) selective growth of dielectric on dielectric. (d) Planarized dielectric with unfilled via, (e) selectively filled with dielectric, and (f) sidewalls selectively coated with metal.

has also led to significant interest for etch stopping applications in the final pattern transfer to the target material.[270–272] Due to the increasing sensitivity to EPE, robust etch stopping for the low-*k* ILD etch is needed to avoid shorting or other reliability issues resulting from unlanded vias. The primary challenge to the implementation of such high-*k* materials as low-*k* ILD etch stopping materials is their potential significant capacitance impact to the metal interconnect.[21] Accordingly, methods for reducing the dielectric constant of high-*k* materials while still maintaining high etch selectivity are needed. One obvious open area of research is the introduction and control of nano-porosity in traditional high-*k* materials to reduce dielectric permittivity as utilized in traditional SiCNH and SiOCH low-*k* etch stop materials.[21,218]

Despite the wide number of materials currently being investigated and available, it is important to note that significant combinatorial based research[36,37] is still needed to sift through the numerous permutations and combinations of materials and etches to find suitable third and fourth color materials. While it is likely that numerous combinations of complementary materials and etches may exist that could represent four unique colors, the many integration requirements that exist for fabricating microelectronic devices may render some material-etch color combinations as unsuitable. Thus, a color technology where numerous off the shelf complementary material-etch colors exist is needed.

Selective Deposition

While new hard mask, spacer, and etch stopping materials may be enabling, they do not significantly reduce the complexity for future pitch division – multi-pattern technologies. One method that has been recently suggested as a means to substantially reduce the patterning complexity is to selectively deposit or grow materials off a previously established pattern template or a pre-existing device or interconnect structure.[273] Such additive bottoms-up processing as opposed to the traditional subtractive top-down method[274] would considerably eliminate the number of litho-etch steps needed to define a transistor or form a metal interconnect structure. At a high level, the matrix of selective deposition capabilities needed is small including just dielectrics on dielectrics, metals on dielectrics, dielectrics on metals, and metals on metals (see Figure 14). Unfortunately, the matrix becomes almost unbounded when the periodic table is added and all the possible combinations and permutations for the desired metals and dielectrics are considered (see Table II).

Fortunately, there is currently no strong preference for the methods by which selectivity may be achieved. Any deposition process including CVD, PECVD, ALD, PEALD, electroplate, sputter, evaporation, and sol-gel spin-on methods may be considered. Further, partially selective processes may also be acceptable in cases where perfect selectivity may be achieved via a repetitive deposition-etch sequence where the etch part is utilized to remove or clean up any partially selective deposition on undesired features.[275–277] Likewise, non-selective deposition processes which yield material properties with significantly different material properties depending on the underlying material or topography could also prove useful in some schemes. Lastly, convert in place strategies may also be considered where standard top-down patterning methods are utilized to form a material pattern that is then converted in place to the desired material. One example of this strategy would be the selective oxidation or nitridation of silicon[278] or a metal[279] surface to form a dielectric metal oxide/nitride such as is currently used in Cu interconnects to improve electromigration.[280–283] A related example would be the recent demonstration of tri-methylaluminum infiltration of organic polymers or surfactants followed by heat-treatment to produce a hybrid organic-inorganic material.[284,285] A final convert-in-place example would be where the top-down patterned material is utilized to catalyze the growth of the desired material. A classic example of this is the vapor-liquid-solid (VLS) mechanism where patterned Au nanodots (~20–40 nm) are utilized to catalytically decompose SiH_4 to grow silicon nanowires.[286,287] In the end, all of the above methods and more may be needed individually or combined to realize future multi-pattern technologies.

However, the requirements for a selective deposition/growth process are quite demanding. As shown in Table III, the need for high yielding processes necessitates that any selective deposition or growth

Table III. Summary of selective deposition requirements for enabling pitch division/multi-pattern processing.

Property	Requirement
Defectivity	Perfect: < 1 ppb (per pass)
Thickness	1 nm–1 micron
Topography	No lateral overgrowth or overhang
Etch Selectivity (wet)	Ability to be removed selectively without damage to others
Etch Selectivity (dry)	Ability to be selectively etched with directionality and bias tuning
Electrical, Optical, Mechanical, Thermal	Same properties and control as non-selective processes
Temperature	< 100–400°C

Table II. Matrix of desired selectively deposited materials and substrates. Note: It is implied that any selective metal or dielectric process is selective against any and all exposed opposing materials.

Template Material/Growth Surface	Selectively Grown Metal/Semi-metal	Selectively Grown Dielectric
Metals/Semi-Metals: Cu, W, Co, Al, Ru, Ti, Ta, TiN, TaN	Cu, W, Co, Al, Ru, Ti, Ta, TiN, TaN	SiO_2, SiN, SiC, Si:H, a-C:H, Al_2O_3, HfO_2, TiO_2, ZrO_2, AlN
Dielectrics: SiO_2, SiNH, SiCH, SiOCH, Si:H, a-C:H, Al_2O_3, HfO_2, TiO_2, ZrO_2, AlN	Cu, W, Co, Al, Ru, Ti, Ta	SiO_2, SiNH, SiCH, SiOC, Si:H, a-C:H, Al_2O_3, HfO_2, TiO_2, ZrO_2, AlN

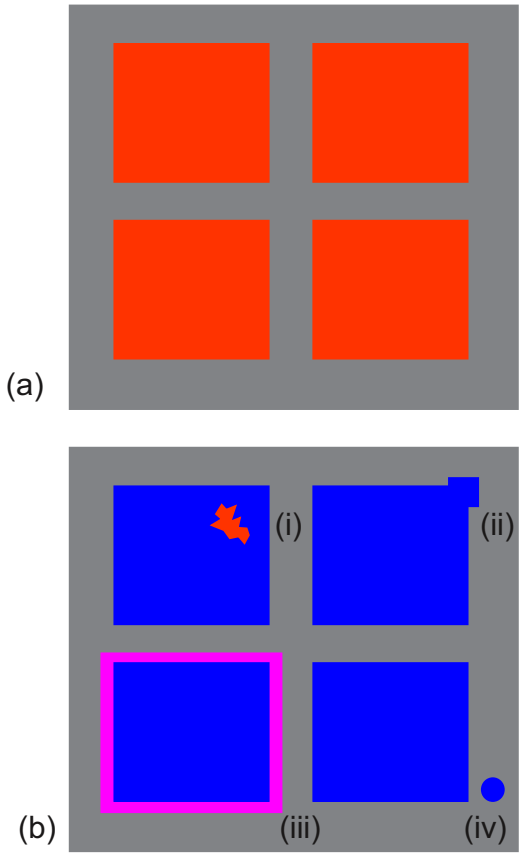

Figure 15. (a) Top-down schematic of a pre-patterned bi-material surface. (b) Selective growth on inlaid material illustrating various types of defects (i) blocked selective growth due to particulate matter or surface contamination, (ii) lateral overgrowth or overhang onto non-selective regions, (iii) attack or corrosion of neighboring non-selective region, and (iv) nucleation and growth on non-selective region.

process have a defectivity of < 1 ppb where the "defects" could represent anything from general particulate contamination, nucleation and growth on undesired features, lateral overgrowth or overhang onto open regions, or etching/degradation of underlying or surrounding exposed materials (see Figure 15).[288] The need for such stringent selectivity requirements is a result of the need to pattern billions of features on a single die and the potential need to use the same selective process on multiple layers leading to additive effects for any defects added or created.[289] The defectivity requirement becomes even more daunting when considering the desired thickness for the selectively deposited material. While in some applications, thicknesses on the order of only a few nanometers may suffice, for many additional applications envisioned, selectively deposited materials with thicknesses more on the order of a micron are desired. In this regard, relatively few of the selective deposition/growth methods demonstrated to date have demonstrated such a high thickness selectivity window with ultra-low defectivity.[38–40,290–292]

The material properties of the selectively deposited material are also critically important. For cases where the selectively deposited material is to be utilized as a photoresist, hardmask, or spacer material, it will need the ability to be etched and selectively removed relative to the other patterning materials using standard dry and/or wet processes.[149,150] Optical transparency and robust mechanical properties are also key considerations. However, for cases where the selectively deposited material will remain to form part of the transistor or interconnect, it will need to additionally have electrical, mechanical, optical, and thermal properties commensurate with the demands of the particular functional layer.[1,11,21] Lastly, deposition/growth temperature is also a significant constraint. For cases where the selectively deposited material is to be grown on or in the presence of photoresist, processing temperatures will need to be limited to $< \sim 100°C$ to avoid polymer melting or relaxation effects.[150] For selective deposition/growth of metal interconnect structures, higher temperatures may be allowed but limited to $\leq 400°C$ to avoid impacting transistor dopant profiles.[21] These temperature constraints, unfortunately, eliminate some selectivity mechanisms popularized for selective epitaxial growth of semiconductors that rely on either differential sticking coefficients or enhanced surface mobility at high growth temperatures.[290,291]

Despite the demanding constraints and challenges, a lengthy list of relevant selective deposition and growth processes have been reported that may be considered for future multi-pattern processes. Selective metals deposition on metals is in fact well known in the industry with numerous reports of selective W, Cu, and Al deposition reviewed in articles by Gladfelter,[38] Hampden-Smith and Kodas,[292] and Amazawa.[293,294] More recent exemplary work covering selective deposition processes for metals and semi-metals such as Co,[295–299] Ru,[300–304] Ni,[305,306] Mn,[307] Mo,[303] Fe,[303,308] Pt,[309,310] and $TiSi_2$[309–311] are summarized in Table IV. The deposition methods utilized to achieve selectivity range from typical dry vacuum CVD and ALD processes[293–296,298–311] to wet electroplating methods.[299,314,315] The former has been typically investigated for contact and diffusion barrier formation as well as contact and via filling.[38] The latter has been investigated for similar applications but recently found more success for selectively depositing metal capping layers on Cu lines to improve electromigration performance.[299]

The selective metals growth can be typically achieved on homo- or hetero-metals as well as metal silicides and Si.[38] The selectivity is typically achieved via native differences in the reactivity between the exposed metal and dielectric surfaces toward the metal precursor. As one example, selective deposition of W on Si or other metals relies on the ability of the Si/metal surfaces to readily catalytically decompose or reduce WF_6 directly via reactions such as:

$$4WF_6 + 6Si \rightarrow 6SiF_4 + 4W, \quad [3]$$

where similar reduction processes do not occur between WF_6 and exposed dielectric surfaces such as SiO_2 and SiN.[38] One challenge to the above reaction, though, is Si consumption which can roughen or degrade the underlying substrate.[316,317] Further, selectivity can also be quickly lost due to side reactions which produce HF and WF_x subspecies that can facilitate metal nucleation and growth on the exposed dielectric surfaces.[318] The surface termination of the dielectric (i.e. presence of hydroxyl species) has also been shown to facilitate metals nucleation directly on the dielectric[319–321]

Regarding selective metals deposition on dielectric surfaces, there have been comparatively fewer reports. However, there have been several recent successes reported, most of which rely on first passivating or deactivating the metal surface with some type of organic or fluorocarbon blocking layer.[39,40] Using such an approach, selective deposition of metals such as Co,[298] Ru[300,322] Ni,[306] Fe,[308] Pt,[309,310,323–325] and TiN[326,327] on dielectric surfaces such as SiO_2, SiN, and HfO_2 have been reported (see Table V). One of the more popular metal surface deactivation methods involves the use of organic self-assembled monolayers (SAMS) which are comprised of relatively long organic alkane chains with reactive groups at both ends.[40] The reactive head group facilitates the adsorption to the desired substrate surface while the tail group either terminates the surface against selective growth or may provide reactive sites for additional selective growth chemistries to nucleate on the SAM. Thiol based SAMs have in particular been widely shown to selectively adsorb onto noble metal surfaces and self-assemble into dense organic layers.[328,329] In this regard, SAMS represent another form of selective deposition and have been previously evaluated as selectively deposited Cu diffusion barriers.[330–332] However, their low thermal stability[331] and similar etch properties relative to photoresists[334] limit their direct utility in multi-pattern processes. Still, these concerns are less of an issue for SAMS and other organic layers as indirect sacrificial blocking layers.

Table IV. Summary of selective deposition on metals. PSG = Phosphosilicate glass, BPSG = borophosphosilicate glass, DODT = 1-dodecanethiol.

Selectively Grown Material	Seed/Template Material	Mask/Selective Growth Against
W[38]	Si, Ta, $TiSi_2$, $TaSi_2$, $CoSi_2$,	SiO_2, SiN, PSG, Al_2O_3, Polyimide
Cu[38,292]	Cu, Pt, W, Co, Mo, Ta, Al, $CoSi_2$, TiN	SiO_2, BPSG, SiN, Polyimide
Al[38,293,294]	Si, Al, Ti, W, Au, TiN, Mo, TiN	SiO_2, SiN, PSG, BPSG
Co[295–299]	Si, Pt, Cu	SiO_2, SiOCH
Ru[301–304]	RuO_x, Pt, Ti, VN, Cu	SiO_2, TiO_2, Al_2O_3, MgO, SiOCH
Ni[305,306]	Ru, Pt	Si, SiO_2, SiOCH
Mn[307]	Cu	SiO_2
Mo[303]	Ti, VN	SiO_2, TiO_2, Al_2O_3, MgO
Fe[303]	Ti, VN	SiO_2, TiO_2, Al_2O_3, MgO
$TiSi_2$[311–313]	Si	SiO_2
Fe_2O_3[386]	Pt	SiO_2
SiCH[387]	Cu	Si/SiO_2
Polyimide[388]	Cu	DODT

In contrast to metals, comparatively fewer selective deposition methods have been reported for traditional dielectrics such as SiO_2 and SiN. For SiO_2, almost all reported methods utilize some type of organic or fluorocarbon blocking layer to achieve selective deposition/growth on either Si, SiO_2, or photoresist. The specific processes span room temperature $SiCl_4/H_2O$ CVD[335,336] to acidic liquid phase deposition methods.[337–341] More recent work has shown the ability to selectively deposit SiO_2 on a wider range of dielectrics (SiO_2, GeO_2, and SiN) using ALD methods and acetylacetone as a chemo-selective growth inhibitor.[342] It should also be noted, semi-selective atmospheric TEOS CVD SiO_2 deposition in conjunction with a SiO_2 etch back has also been utilized to achieve a selective SiO_2 process.[277] For SiN, the authors are aware of only the work by Yokoyama where a SiH_2Cl_2/NH_3 ALD process was reported with the ability to grow 4 nm of SiN selectively on hydrogen terminated Si relative to a higher temperature/lower hydrogen content LPCVD SiN film.[343]

For high-*k* dielectrics, there have been significantly more reports of selective deposition on Si and dielectrics utilizing almost exclusively ALD methods. Many of the reports of selective high-*k* growth rely on native differences in the surface chemistry/reactivity between hydroxylated silicon/SiO_2 (Si-OH) and metal oxide surfaces versus hydrogen terminated Si or metals.[344–351] Unfortunately, these methods typically have a thickness window of < 1 nm before selectivity is lost and nucleation on the non-growth surface becomes significant. However, Atanasov[345] and Longo[351] have shown that the selectivity window is dependent on the ALD oxide with selective thicknesses up to 2 nm being achieved for TiO_2. Still higher thickness selectivity windows have been achieved using again various organic and fluorocarbon blocking layers.[352–359] In fact, Reinke et al.[355] have reported up to 99 ± 5 nm of TiO_2 selectively grown on Si with a perfluorodecyltrichlorosilane blocking layer.

The thickness selectivity window for blocking layer approaches, however, is quite sensitive to both the type of material utilized and the ALD chemistry for both metals and dielectrics.[40] In particular, Sinha has shown that sorption, reaction and diffusion of the ALD precursors into the organic blocking layer can be a key limiter to the thickness selectivity window which is dependent on both the density/packing efficiency of the blocking layer and the specific ALD precursors.[360–362] Hughes has further shown that wildly different results can be achieved for the same blocking layer with different ALD chemistries where a polyethlyeneimine (PEI) blocking layer was completely ineffective for selective Al_2O_3 growth but showed good growth attenuation for ALD Ta_2O_5, HfO_2, and TaN.[363] Similarly, Zhang[364] and Hashemi[365] have shown that the substrate material and SAM deposition method can have a significant effect on the SAM blocking layer formation. Specifically, Zhang found that the thermal stability and TaN ALD blocking ability for two different fluorinated alklysilane SAMS is different when deposited on SiO_2 versus Cu. Hashemi has established that vapor deposited alkanethiol SAMS are more effective than solution deposited SAMS for blocking ZnO and TiO_2 ALD. For high

Table V. Summary of selective deposition on dielectrics. PSG = Phosphosilicate glass, BPSG = borophosphosilicate glass. OTS = Octadecyltrichlorosilane, PMAM = Polymethacrylamide, PR = photoresist, ODPA = octadecylphosphonic acid, MUO = 11-mercapto-1-undecanol.

Selectively Grown Material	Seed/Template Material	Mask/Selective Growth Against
Co[298]	SiO_2	OTS
Ru[300,322]	SiO_2, HfO_2, SiCN	OTS, a-C:H
Ni[306]	SiO_2	OTS
Fe[308]	SiO_2	W
Pt[309,310,323–325]	Si, SiO_2, ZrO_2	PMAM, CF_x, OTS
TiN[326,327]	HfO_2, Si_3N_4	a-C:H
SiO_2[335–337,342]	Si, SiO_2, SiN, GeO_2, W, WO_3, PR	SiO_2, CF_x, PR, Al_2O_3, TiO_2, HfO_2
SiN[343]	Si(H)	SiN
TiO_2[326,344–346,355–357]	Si-OH, SiO_2, SiN	Si-H, Cu, a-C:H, CF_x, PMMA
HfO_2[327,347,348,352–354]	Si-OH, SiO_2, SiOCH, SiN	Si-H, Cu, OTS, a-C:H
ZrO_2[349,353]	Si-OH, SiO_2	Si-H, Cu, OTS
Al_2O_3[357,358]	Si-OH	PMMA, OTS
Hf_3N_4[358]	SiOCH	OTS
Polymeric C[370–378]	Si/SiO_2, MUO	OTS, ODPA, Cu, Ru, Fe, Pt
Si:H[275]	Si	SiO_2
pc-Si[379,380]	Si, SiO-OH	SiO_2

Table VI. Summary of characteristics for resistive switching devices demonstrated using CVD, PECVD, and spin-on silicon-based dielectrics commonly utilized in CMOS device and metal interconnect fabrication.

Electrolyte Material	Inert/Active Electrodes	Unipolar/ Bipolar	V_{on}, V_{off} (V)	R_{on}/R_{off}	Endurance (# cycles)	Retention
PECVD SiO_2[636–639]	Au, Pt, TaN/Cu	Biploar	0.2–1, −0.2––0.5	100–1000	>200	$>10^4$ sec (@ 85°C)
PECVD SiO_x ($x = 1$–2)[640–644]	W, Pt/Cu	Unipolar	5, 1	100 - 10^4	>60	$>10^4$ sec (@ 100°C)
PECVD SiO_x ($x = 1$–2)[640–644]	W, Pt/Cu	Bipolar	1, −2	100 - 10^4	>60	$>10^4$ sec (@ 100°C)
Spin-on SiOCH[645–647]	W, Pt/Cu, Ag	Bipolar	0.7, −0.15	$>10^4$	500–2000	$>10^3$ sec (@ 85°C)
PECVD SiOCH[635]	W, Pt/Cu, Ag	Bipolar				
LPCVD SiN_x:H ($x \cong 1.3$)[649–651]	Si/Ni, Au	Bipolar	4, −2	10–10^5	50–100	$>10^4$ sec (@ 100°C)
PECVD SiN_x:H ($x = 0.6$–1.2)[651–655]	W, Al, Pt/Ag, Ti, Ni	Bipolar	1–2, −1––2	70–10^3	$>10^3$	$>10^5$ sec (@ 85°C)
SiC_x:H ($x \cong 1$)[659–664]	Pt, Au, W/Cu, Ag	Bipolar	1–2, −1––2	100–10^8	$>10^4$	$>10^4$ sec (@ 85°C)
Polymer ($x = 1$ - > 3)[665–669]	Ru, Ta/Cu	Bipolar	2–3, −1––1.5	10^3–10^5	$>10^5$	$>10^4$ sec (@ 150°C)
a-Si:H[670–675]	Si/Ag, Ti	Bipolar	3–5, −1––3	>100	$>10^3$	$>10^4$ sec (@ 150°C)

thickness selective growth, an additional concern using SAM blocking layers is their low thickness of 1–2 nm[327] which may allow lateral overgrowth of the selectively grown material onto the SAM to occur and thus eventual loss of pattern fidelity and selective growth.[40,366] In this regard, Prasittichai[367] and Closser[368] have shown that this effect in some cases can be minimized by either utilizing a wet etch or an electrical bias, respectively, to selectively desorb the SAM and take the laterally overgrown material with it.

It is also possible to utilize SAMS and other selectively formed organic layers directly as nucleation layers for selective growth. This approach has been demonstrated by Jeon[325,369] and others[370–373] for selectively growing various polymer films relative to Si, SiO_2, and other organic layers. In this approach, the terminal end of the SAM contains a reactive end group that acts as a seed site for the incoming CVD or ALD chemistry to nucleate and grow directly on the SAM.[373] Selective growth of such polymers has been reported using SAMS as blocking layers[374,375] as well as metals, metal salts, and organometallic complexes such as those of copper, ruthenium, iron, and platinum.[376–378]

We do also note that amorphous and poly-crystalline (pc) Si in many cases is utilized as a hard masking or other type of sacrificial patterning material.[242,243] In this regard, there have been a few reports of selective a-Si:H[275] and pc-Si.[379,380] For the former, periodic hydrogen etches are utilized to remove partially selective PECVD a-Si:H from non-growth regions. It has been reported that the length of the deposition and etch times can be tuned to achieve selective deposition on Si, SiO_2, and metals.[275] The hydrogen etch, however, may be incompatible with multi-pattern processes where photoresist exists. Similarly, Miyazaki[378] and Jung[379] have reported on the selective deposition of Si on SiO_2 using high temperature (560–850°C) CVD. While this may again be too hot for many multi-pattern and interconnect processes, it may be useful for early FEOL patterning or to allow convert in place strategies to other useful materials such as SiN or metal silicides.

Lastly, it is worth also mentioning photo or laser-assisted CVD and ALD methods as potential selective growth process. Numerous reports reviewed in articles by Hanabusa,[381] Allen,[382] Donnelly,[383] Fang,[384] and Chalker[385] have demonstrated the ability to direct write both metals and dielectrics on a variety of surfaces using broadband sources or lasers operating at wavelengths spanning the IR-visible-UV range. While these methods may be slow and not likely to alleviate alignment/edge placement issues in multi-pattern processes, they could still prove useful for direct writing of low-density anchor patterns to seed the selective growth of other materials and structures. One direct analogy would be graphoepitaxial methods utilized in the directed self-assembly (DSA) of block copolymers where course topographic patterns are utilized to guide the phase separation into desired nano-structures.[386]

Despite the significant amount of research demonstrating a vast array of selective deposition processes, significant dielectrics related research in this area is still needed. One clear gap concerns selective deposition of dielectrics on metals (see Table IV). Aside from the growth of native metal oxides on metals, the authors are aware of only a handful of reports demonstrating selective deposition of a dielectric on relevant metals such as Cu.[387–389] The range of reported dielectrics deposition processes selective to either metals or dielectrics is also somewhat limited to primarily high-*k* dielectric materials (see Tables IV and V). For most applications where the dielectric will remain in the final formed structure, low-*k* SiO_2, SiN:H, SiOC:H, SiCN:H, and SiC:H dielectrics would be preferred.[9,21] Thus, significant research is needed to expand both the composition space of selectively deposited materials and the substrates on which selectivity can be achieved.

In addition, significant research is needed to develop defect mitigation strategies to further improve the inherent selectivity for the previously demonstrated selective processes and to significantly expand their thickness process window for maintaining selectivity. While organic passivation/blocking layer strategies may be utilized, there is a strong preference for processes which capitalize on native pre-existing surface and material heterogeneities to achieve selectivity and therefore minimize the number of processing steps needed and ultimately cost. All of the above would be greatly aided by developing uniform methods for quantifying and modeling selective growth processes.[390]

High-*k* and Low-*k* Dielectrics: What Was Old Becomes New Again

Beyond enabling lithography and single digit nm patterning methods, low-*k* and high-*k* dielectric materials are re-emerging in a host of new applications. High-*k* materials in particular continue to be of research interest in their traditional role as a gate dielectric material but in conjunction with other semiconducting materials such as wide bandgap semiconductors for high-power, -frequency, and -temperature applications;[391–394] organic polymer semiconductors for flexible electronics,[395,396] and amorphous and poly-Si thin film transistors (TFT) for flat panel display applications.[397,398] Use of the ALD Al_2O_3 precursor tri-methyl aluminum (TMA) has also been shown to be useful for "self-cleaning" of the native oxide of the III-V semiconductor GaAs.[399] In particular, Lee, et al. showed that 4 TMA pulses at the beginning of ALD Al_2O_3 deposition led to a reduction of As oxides below the XPS detection limit, and significantly decreased Ga oxide concentration.[400] This method of native oxide removal allows for in-situ targeted native oxide removal under vacuum prior to dielectric deposition. Thermal and plasma-enhanced atomic layer deposited (PEALD) Al_2O_3 has additionally been used in high-efficiency solar cells to passivate the back side of p-type Si solar cells such that surface recombination rates are reduced.[401,402] Al_2O_3 is uniquely suited for this application as it passivates via negative fixed charge at the Si surface while ALD allows for deposition of very thin, conformal layers of Al_2O_3.

Due to their varied chemical, mechanical, electronic, magnetic, and physical properties, high-κ materials are finding use in

even wider ranging applications. One such example is the use of $Hf(OH)_{4-2x-2y}(O_2)_x(SO_4)_y{\cdot}qH_2O$ ($HfSO_x$)[403–405] and related metal oxide materials[406,407] as inorganic photoresists for extreme UV (EUV) patterning. The high elastic modulus[7] and corrosion resistance[408] of high-*k* oxide and nitrides have additionally made them of interest as stiction prevention, frequency tuning, and movable/resonating materials in micro/nanoelectromechanical devices.[51,52,409–411] Further, the high hardness[7] and chemical inertness[412] of high-*k* oxides makes them of interest for numerous tribological[413,414] and protective antibacterial[55,56,415] and moisture encapsulation[416,417] coating applications. The high refractive index and optical transparency[7] of high-*k* oxides also makes them of interest in waveguide and optical coating applications.[418–420] High-*k* oxides are even of interest for various gas pressure[421] and chemical sensors[53,422–424] applications due to the significant ionic conductivity and defect chemistry exhibited by materials such as ZnO, TiO_2, ZrO_2, and HfO_2.[425]

The role of high-*k* materials has also continued to expand in more traditional logic and memory device applications. As one example, the recent discovery of ferroelectric[47,48] and ferromagnatic[426] properties in HfO_2 and related high-*k* dielectrics has created substantial interest in memory applications[46,49,427,428] and negative (differential) capacitance transistor devices as a means for further extending CMOS device scaling.[44,45,429]

High-*k* materials are also finding use in metal/insulator/metal (MIM) back-end-of-line (BEOL) structures such as decoupling capacitors[430] and resistive random-access memory devices,[41] and in metal/insulator/semiconductor (MIS) configurations as Fermi-level de-pinning layers. High-*k* MIM devices are further emerging as high speed MIM tunnel devices for applications such as rectifying antennas (rectennas). The benefit of high-κ materials for these latter four applications will be examined in more detail below.

Metal-Insulator-Metal Capacitors with High-κ Insulators

MIM capacitors have become a core passive component in most integrated circuits (IC). Applications using MIM capacitors include analog-to-digital converters (ADC), analog noise filters, DC voltage decoupling, electrostatic discharge (ESD) protection, and dynamic random-access memory (DRAM).[431–433] Initially analog and mixed signal (AMS) ICs used metal-insulator-silicon (MIS) capacitors, but these were quickly replaced by polysilicon-oxide-polysilicon (double-poly) capacitors for their improved voltage nonlinearity.[434,435] Double-poly capacitors were subsequently replaced by MIM capacitors due to the shift into multi-gigahertz frequencies. MIM capacitors showed reduced resistive losses, further improved voltage nonlinearity, reduced parasitic capacitance, increased capacitance density, and increased quality factor.[436,437]

MIM capacitors are found in the back end of line (BEOL) interconnect layers, reducing the need for discrete off-board components and enabling decreased metal trace lengths. This increase in integration has led to increased device packing density and decreased transmission delay. Continued increases in packing density and scaling of devices requires increasing capacitance density (see Eq. 1) which may be achieved either through reducing the dielectric film thickness (t_{ox}) or integrating higher dielectric constant (κ) materials. However, decreasing the dielectric film thickness causes undesirable increases in both leakage current density and the quadratic voltage coefficient of capacitance (αVCC), where αVCC is a value obtained from empirical modeling of the capacitance-voltage (CV) behavior using[438]

$$\Delta C/C_0 = (\alpha VCC)\,V^2 + (\beta VCC)\,V, \qquad [4]$$

where C_o is the value of the capacitance at 0 V, ΔC is the change in capacitance as a function of voltage, and βVCC is the linear coefficient. While the αVCC is not necessarily an important parameter for BEOL DRAM capacitors, it is a critical parameter for RF AMS capacitors. The fundamental origin of the voltage non-linearity of capacitance is still under debate. Mechanisms that have been proposed for αVCC include non-linear metal-oxygen bond polarizability,[439,440] dielectric thermal expansion,[441] free carrier injection into oxygen vacancies creating a double layer,[442–446] induced film strain from electrostriction and Maxwell stress,[447–449] interfacial layer oxides (ILOs) formed at each metal-insulator interface,[442,443,450–452] and lattice mismatch between the insulator and each metal.[450]

High-κ dielectrics were first investigated in MIM capacitors for scaling of DRAM. The goal was to enable decreased device cell areas and increased packing density by increasing capacitance density. Achieving the required capacitance density with SiO_2 or Si_3N_4 required reducing film thickness to only a few 10's of Å, which caused undesirable increases in leakage current due to direct tunneling as well as increases in αVCC. It was found that for device requirements of the early 2000's, implementation of alternative high-κ materials was less cost efficient than integrating thicker films of SiO_2 and Si_3N_4 within high aspect ratio structures, such as trench and stacked capacitors (MIMIM).[451] As a result, SiO_2 and Si_3N_4 remained the primary dielectrics in MIM capacitors with κ values of 3.9 and 7, respectively.[1] However, industry interest in alternate thin film high-κ dielectrics continued due to ever increasing capacitance density requirements. Many alternative high-κ insulators have been studied including Al_2O_3,[452,453] $AlTiO_3$ (ATO),[454–455] (Ba,Sr)TiO_3 (BST),[456–459] BiTaO,[460] (Bi,Ti)SiO_3 (BTSO),[461] HfO_2,[462] HfSiO,[463] La_2O_3,[464] Sm_2O_3,[465] $SrTiO_3$ (STO),[457,466–469] Ta_2O_5,[470,471] TiO_2,[455,472] Y_2O_3,[473,474] and ZrO_2.[475–477]

The International Technology Roadmap for Semiconductors (ITRS) 2026 projections for MIM capacitors indicate a need for low equivalent oxide thickness (EOT) values near 1 nm while maintaining low leakage currents of 10^{-8} A/cm^2. Alternative dielectrics with κ values of at least 40 are needed to meet the EOT requirement. However, high-κ values correlate with decreased dielectric breakdown strength (E_{bd}), with a relationship of $E_{bd} \sim (\kappa)^{-1/2}$, and increased αVCC.[478,447]

Several high-κ dielectrics are of interest as candidates for meeting IRTS projections. HfSiO is close to the required κ with a relatively large bandgap and has already been studied for use in transistor gate stacks. Al_2O_3 has a large bandgap and a high crystallization temperature but has only a moderate κ and larger αVCC.[479] These properties may make Al_2O_3 promising for use in a transitional period or within a multi-layer dielectric stack. Materials from ternary structural families such as ABX_3 and ABX_4, including STO, BST, BTSO, and $BiTaO_4$, tend to have very large κ values, but higher leakage. Finally, multicomponent films containing Bi_2O_3 have displayed large κ values with processing temperatures well below BEOL thermal budget limits.

However, despite extensive research, no single dielectric has yet been determined to be capable of meeting all the ITRS requirements for MIM capacitors. Instead, nanolaminate stacks of two or more dielectrics may be the key to simultaneously achieving high capacitance density with low leakage and low voltage nonlinearity. An additional benefit of the multilayer dielectric technique, as reported by Ding et al., is that increasing the number of layers has the ability to interrupt grains and reduce leakage currents.[480] It is important to note that each layer in a nanolaminate acts as a capacitor in series and thus the lowest κ material will dominate the overall capacitive behavior of the system. Nanolaminates of Al_2O_3 and ZrO_2 (ZAZ) have been shown to have high capacitance density with reduced leakage. However, ZAZ devices display large voltage nonlinearity due to each dielectric having a positive (+)αVCC.[481] The majority of dielectrics have a (+)αVCC which tends to increase with increasing κ. A few, however, have been found to have negative (-)αVCC, such as BST, SiO_2,[482] STO, TiO_2, and ZrTiO.[483] Examples of CV behavior for a (+)αVCC dielectric (Al_2O_3) and a (-)αVCC dielectric (SiO_2) are shown in Figure 16. As shown by Kim et al., combining a (-)αVCC dielectric with a (+)αVCC dielectric leads to a considerable reduction of the overall effective αVCC of the device, known as the cancelling effect.[484] Creating a nanolaminate using one high-κ dielectric with a (+)αVCC and another high-κ dielectric with a (-)αVCC, one of which is amorphous in order to reduce the leakage current, is one of the most promising techniques to realize ITRS goals.[484,485]

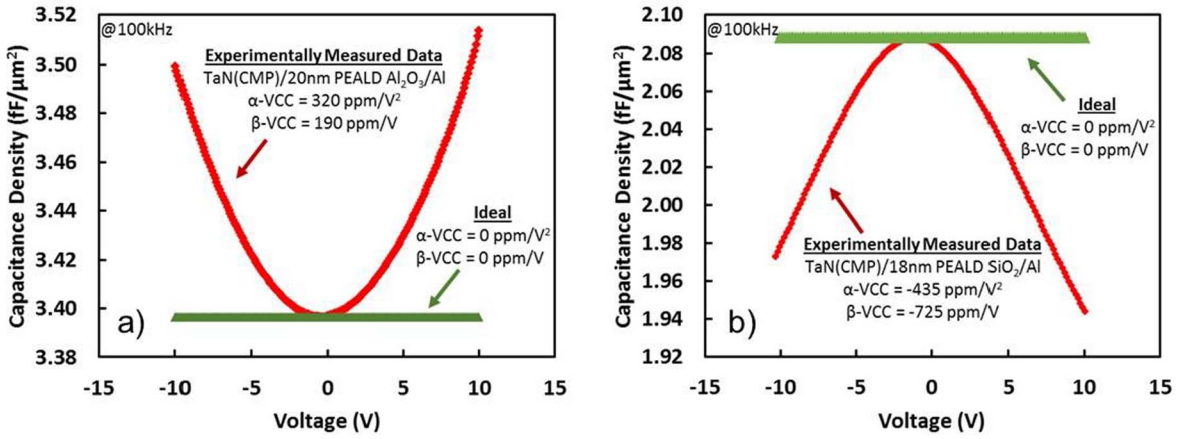

Figure 16. (a) Capacitance-voltage (CV) behavior for plasma enhanced ALD (PEALD) Al_2O_3 in red, demonstrating (+)αVCC, as compared to an ideal CV curve in green. (b) Capacitance-voltage (CV) behavior for plasma enhanced ALD (PEALD) SiO_2 in red, demonstrating (-)αVCC, as compared to an ideal CV curve in green. Adapted from Ref. 484.

Fermi Level De-Pinning

In an ideal metal-semiconductor (MS) contact, there are assumed to be no interface states or chemical interactions between the two materials. When separated, the bands of both materials are ideally flat and are referenced to the vacuum level (E_{vac}), which is taken to be the energy of a free electron just outside of the surface. The metal is defined by its work function (Φ_M), the energy difference between the Fermi energy (E_F) and E_{vac}. The semiconductor is defined by the electron affinity (χ_S), the difference between the conduction band minimum, E_C, and E_{vac}. When brought together, the Fermi levels of the two materials align, causing the conduction and valance bands of the semiconductor to bend along with the local vacuum level, $E_{vac,local}$. As a result, a Schottky barrier, φ_{Bn}, forms between the two materials, as shown in Figure 17. In the simplest model, charge transfer across the interface is neglected, and φ_{Bn} is predicted to vary with the vacuum work function of the metal ($\Phi_{M,vac}$), according to the Schottky-Mott rule[486] where

$$\varphi_{Bn} = \varphi_{M,vac} - \chi_S, \quad [5]$$

However, this ideal Schottky-Mott behavior is not typically observed.[487–490] In real devices, Φ_M often does not have as strong of an influence on φ_{Bn} as predicted. This is a deviation historically referred to as Fermi-level pinning.[491,492]

The most widely accepted theory for the cause of pinning is the presence of interface states, both due to physical defects and virtual metal-induced gap states (MIGS). MIGS arise from a quantum mechanical behavior of electrons at the metal surface. The electrons in a metal have defined wave functions, and at the surface of the metal these wave functions decay exponentially. When the surface of the metal is instead an interface with an insulator or semiconductor, the wave functions decay into that material, creating available virtual states at the interface within the forbidden gap.[491]

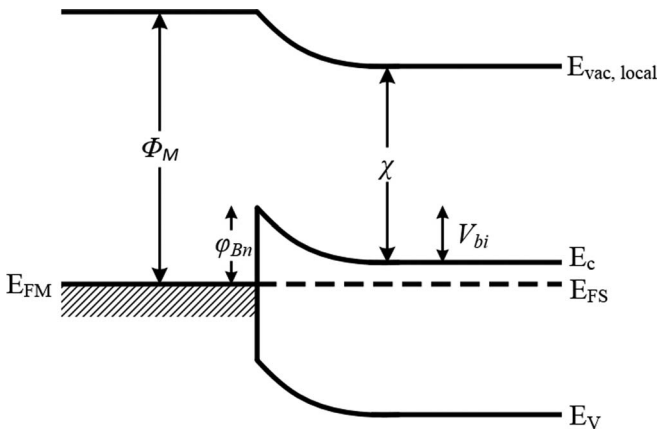

Figure 17. Ideal band alignment for a metal-semiconductor contact.[6,491]

In MIGS theory, charge transfer at *induced* or *intrinsic* interface traps creates an interfacial dipole that drives the metal Fermi level (E_{Fm}), toward the charge neutral level of the insulator ($E_{CNL,i}$), the energy at which the dominant character of the interface states in the forbidden gap switches from donor-like to acceptor-like.[490,493] Thus, the metal behaves as if it has an effective work function, $\Phi_{M\text{-}eff}$, different from $\Phi_{M,vac}$, where:

$$\Phi_{M,eff} = E_{CNL,i} + S\left(\Phi_{M,vac} - E_{CNL,i}\right) \quad [6]$$

and where S is the slope parameter defined as the slope of a plot of φ_{Bn} versus $\Phi_{M,vac}$ for a given semiconductor or insulator,

$$S = \frac{\partial \varphi_{Bn}}{\partial \Phi_M}.^{492} \quad [7]$$

The degree of pinning at a metal-semiconductor or metal-insulator interface is characterized by S which describes how much $\Phi_{M\text{-}eff}$ actually changes in response to a change in $\Phi_{M,vac}$. $S = 0$ indicates the limit of complete "pinning" of E_{Fm} at $E_{CNL,i}$, while $S = 1$ indicates the opposite limit of no pinning.

Mönch found an empirical relationship between the S factor and the electronic dielectric constant (ε_∞) where[492]

$$S = \frac{1}{1 + 0.1(\epsilon_\infty - 1)^2}. \quad [8]$$

This relationship between the degree of pinning and ε_∞ shows that high-κ materials, including Si itself, will tend to have a smaller S value than low-κ materials, indicating stronger pinning. Despite the success of MIGS theory, it can be difficult to calculate or determine the E_{CNL} for a given material and it is often observed that φ_{Bn}'s can deviate substantially from predictions due to *extrinsic* defects that can arise from processing details such as deposition method, interface traps and near interfacial trapped charge due to point defects such as E' and P_b centers,[178,493–497] dipoles due to interfacial chemical reactions, interfacial oxide layers,[498] and remote scavenging of oxygen.[499,500]

An understanding of these mechanisms and the ability to control them becomes very important when looking to use metal electrodes as a contact for semiconductors. Work by Connelly et al. showed that insertion of a thin layer of Si_3N_4 decreased the Schottky barrier height via reduction of Fermi-level pinning.[487] Nishimura et al. then demonstrated similar control of the metal/Ge barrier height with insertion of a thin dielectric layer.[501] These works and others have shown that depinning of metal-semiconductor interfaces may be achieved through

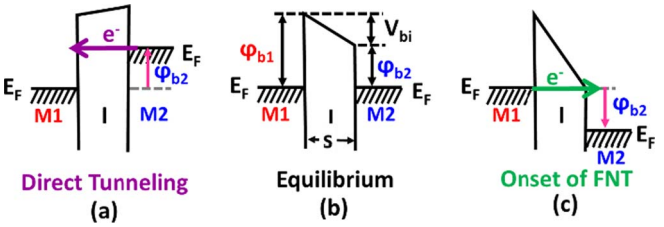

Figure 18. Band diagrams of dissimilar work-function MIM device with M1 at ground illustrating (a) direct tunneling under negative bias ($-\varphi_{b2}$) applied to M2, (b) equilibrium, and (c) Fowler-Nordheim tunneling (FNT) under positive bias ($+\varphi_{b2}$) applied to M2.

addition of a thin dielectric at the metal-semiconductor interface.[487,502] As described below, it is therefore necessary to directly measure φ_{Bn} for each metal/insulator combination with a technique such as internal photoemission spectroscopy (IPE).

MIM Tunnel Diodes

MIM diodes comprise a simple structure consisting of a thin insulator between two metal electrodes. Most of the original work on MIM tunnel devices was performed using point contact devices in which the top contact was made mechanically, typically with a tungsten needle, resulting in unstable operation and low reproducibility.[503–505] More suitable for mass production, thin film MIM based tunneling devices have seen increased interest for a number of high speed applications,[76,506–516] including tunnel diodes for optical rectifying antenna (rectenna) solar cells for infrared (IR) energy harvesting,[517–527] building blocks for MIMIM hot electron transistors,[528–535] single electron transistors,[536] and infrared (IR) detectors.[537–542] Other applications include selector diodes for resistive random-access memory (RRAM),[6,534] and MIM tunnel emission cathodes.[543–547] Finally, because of their simple fabrication and potential for low temperature processing on large area glass and flexible substrates MIM structures have been proposed for use in large area macroelectronics such as liquid crystal display (LCD) backplanes.[548,549]

Operation of MIM diodes is based on quantum mechanical tunneling,[550–552] potentially allowing operating speeds of greater than one terahertz.[553,554] Figures of merit for rectenna applications include current asymmetry ($\eta_{asym} = I^-/I^+$), zero-bias responsivity ($\Re = \frac{1}{2}(d^2I/dV^2)/(dI/dV)$), and zero bias resistance. High η_{asym} and $\Re$, and low ZBR and turn-on voltage (V_{ON}) are desired. All of these arise directly from the structure. A symmetric structure having a single insulator and similar work-function (Φ_M) top and bottom electrodes would have equal probabilities for electrons tunneling in opposite directions. On the other hand, a device with dissimilar work-function electrodes ($\Phi_{M1} \neq \Phi_{M2}$) produces a built-in voltage ($V_{bi} = (\Phi_{M1} - \Phi_{M2})/e$, where e is the electronic charge) across the tunnel barrier and obvious asymmetry (see Figure 18) leading to different probabilities for electrons tunneling in opposite directions.[555,556]

Operation of these diodes is based on Fowler-Nordheim tunneling (FNT), described in Eq. 9:

$$J_{FNT} = C_1\left(\frac{V+\Delta\varphi_b}{S}\right)^2 exp\left(-C_2\sqrt{m^*}\varphi_b^{\frac{3}{2}}\left(\frac{S}{V+\Delta\varphi_b}\right)\right) \quad [9]$$

where J_{FNT} is current density, V is the applied voltage, $\Delta\varphi_b$ is the difference in electron barrier heights (φ_{b1}-φ_{b2}) between the bottom and top electrodes (M1 and M2, respectively), S is the thickness of the insulator, m^* is the effective mass for tunneling, and C_1 and C_2 are constants. It is seen that J_{FNT} depends exponentially on φ_b, m^*, and the electric field (V/S).[546,549] Because S will typically be much less than 10 nm, minimizing metal/insulator interfacial roughness is critical for electric field uniformity. Early thin film diode work was performed mostly using native oxides grown on polycrystalline metal bottom electrodes.[505,508,509,512,513,533–537,557–563] The roughness of these electrodes was typically much greater than the thickness of the insulator, meaning that the I-V characteristics of these devices were often likely dominated by random "hot spots" due to electric field enhancement.[564–566] Techniques such as atomic layer deposition (ALD) now allow for the deposition of high-quality insulators, independent of the bottom metal electrode.[567–569] Work on ALD Al_2O_3 MIM devices has demonstrated that roughness can dominate device operation and that reducing roughness leads to predictable I-V characteristics, and improved uniformity and yield.[76] More recent work has quantified the impact of electrode roughness on tunneling.[570] Ultrasmooth amorphous metals,[571,572] have been shown to be beneficial for transistor operation.[573,574] The amorphous metal ZrCuAlNi has been shown to improve MIM device operation and yield.[507,575,576] However, the sensitivity of ZrCuAlNi to oxidation[577] has led to the development of new thin film amorphous metals such as TaWSi and TaNiSi.[578,579] Further development of amorphous metals will increase options for engineering MIM devices. It should be noted that through intentional control of electrode geometry, the "lightening rod" effect field-enhancement, including the use of carbon nanotubes (CNTs) has been exploited to improve asymmetric operation.[509,524,527,580–582]

MIM diode performance can be engineered by both the metal electrodes and the insulator. For the electrodes, the maximum induced V_{bi} is limited by the roughly 1 eV or so maximum $\Delta\Phi_M$ that can be achieved using practical metals.[548,583] Insulator properties, including bandgap (E_G), electron affinity (χ_I), and metal/insulator electron barrier heights (φ_{Bn}) are critical in determining MIM diode performance and suitability for a particular application. For a diode, there are competing requirements. V_{ON} and low ZBR can be reduced by using a thin film (less than 10 nm) and choosing a material with a narrow E_G or larger χ_I to form a low tunnel barrier. High maximum η_{asym}, however, is favored by a wider E_G or smaller χ_I. If the insulator is too thin, then direct tunneling will play a greater role in charge transport, reducing η_{asym}. For high speed, stable, asymmetric, and temperature insensitive operation, conduction through the insulator should be dominated by FNT. In addition, conduction in narrow E_G insulators with small φ_{Bn} are often dominated by thermionic emission mechanisms such as Schottky and/or Poole-Frenkel emission due to high densities of shallow defects.[76,583] Although defect density may be reduced either through post deposition annealing, substrate and bottom electrode temperature sensitivity may prevent optimization. Finally, as RC time constants may also limit switching speed, a high κ is undesirable.

Precise knowledge of φ_{Bn}'s is critical for predicting, understanding, and optimizing MIM charge transport and operation. As described above, in the simplest model, φ_{Bn}'s are estimated from the vacuum properties of the materials (the vacuum work function of the metal, $\Phi_{M,vac}$, and χ_i), according to Schottky-Mott, $\varphi_{Bn} = \Phi_{M,vac} - \chi_i$.[486] In practice, it is observed that actual φ_{Bn}'s depend on deposition methods and processing and can deviate substantially from this simple expression due not only to intrinsic induced gap states, interfacial dipoles, and Fermi level pinning, but also to extrinsic interface traps and near interfacial trapped charge due to point defects, dipoles due to interfacial chemical reactions, and remote scavenging of oxygen. It is therefore necessary to directly measure φ_{Bn} for each metal/insulator combination. The best technique to directly measure barrier heights "in-situ" (in device structures) is internal photoemission spectroscopy (IPE).[488,585,586] Though most work to date has involved MOS structures, there have recently been a few reports of IPE measurements of both top and bottom metal/insulator barrier heights within MIM devices.[587–589] Direct IPE measurements of φ_{Bn} are also needed in assessing the impact of high-k materials used to "de-pin" metal-semiconductor contacts (discussed in the previous section), as well as for high-k materials used as gate dielectrics for Si and other semiconductors.

A number of thin film single insulator MIM diode systems have been investigated.[76,506–512,517–521,524,526,537–540,581,590–597] Despite this extensive work on MIM devices, the traditional approach of using dissimilar metal electrodes to achieve rectification is limited by $\Delta\Phi_M$ and by the properties (φ_{Bn}'s and charge transport mechanisms) of the single insulator. For example, while narrow E_G insulators may suffer from thermionic based conduction and higher dielectric constant,

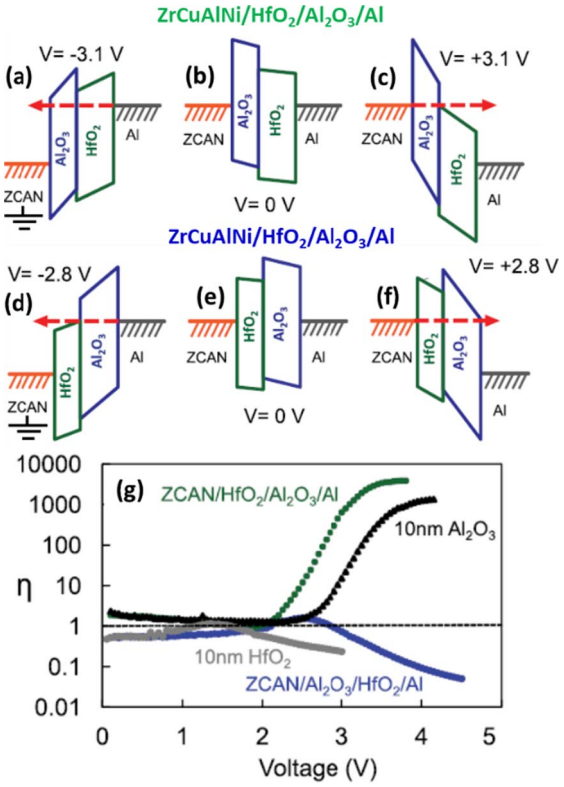

Figure 19. Band diagrams of $ZrCuAlNi/HfO_2/Al_2O_3/Al$ and $ZrCuAlNi/Al_2O_3/HfO_2/Al$ MIIM devices showing equilibrium (b, e), direct tunneling (a,f), and step tunneling (c,d). (g) Plots of asymmetry ($|\eta_{asym}|$) vs. voltage for both MIIM devices as well as single insulator $ZrCuAlNi/Al_2O_3/Al$ and $ZrCuAlNi/HfO_2/Al$ MIM devices. Adapted from Refs. 515,521.

wide E_G insulators may be limited by high V_{ON} and high zero bias resistance. An alternate way to create asymmetry is using the tunnel barrier itself. Theoretically, formation of an asymmetric tunnel barrier can be accomplished using stacked nanolaminate insulator heterostructures.[598–602] As shown in Figure 19, pairing insulators having different E_G and χ_i allows for the formation of highly asymmetric tunnel barriers.[516,522] Equilibrium band diagrams in Figs. 19b and 19e illustrate the built-in field (V_{bi}) induced by the dissimilar workfunction ZrCuAlNi and Al bottom and top electrodes.

For MIIM diodes in which each insulator in the pair is dominated by tunneling based conduction, asymmetry may be improved over that of single insulator MIM diodes either by step tunneling (ST) or resonant tunneling (RT). Step tunneling (see Figs. 19c and 19d) occurs when electrons tunnel through only the wide E_G insulator (here Al_2O_3) into the conduction band of the narrow E_G insulator (in this case HfO_2). For the opposite polarity but same magnitude bias, (see Figs. 19a and 19f, respectively) electrons must tunnel through both dielectrics, leading to lower tunneling probability and asymmetric operation.

It is critical that the asymmetry induced by the asymmetric tunnel barrier aligns with the asymmetry induced by the electrodes through $\Delta\Phi_M$. As seen in Fig. 19g, when the asymmetry induced by step tunneling aligns with that produced by $\Delta\Phi_M$ (Fig. 19c), η_{asym} may be increased and V_{ON} reduced (green circles) over a single layer Al_2O_3 MIM (black triangles). If the insulator stack order is reversed so that the step tunneling induced asymmetry opposes $\Delta\Phi_M$ (Fig. 19d), η_{asym} may be reduced or even reversed (blue squares in Fig. 19g). This work demonstrates that barrier engineering is a more powerful and effective way to engineer asymmetry in MIIM devices than $\Delta\Phi_M$. Resonant tunneling (RT) is another mechanism by which dual insulators may improve asymmetry.[513,519,603–608] In resonant tunneling (RT), electrons transport via FNT through the lower E_G insulator to a quantum well formed between the two insulators followed by FNT through

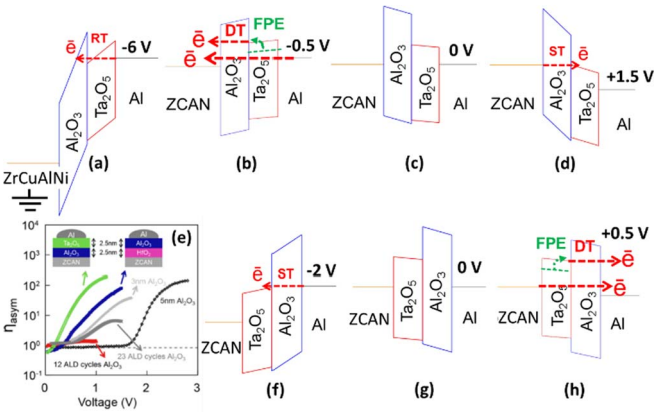

Figure 20. Band diagrams Adapted from Ref. 507.

the second insulator (see Figure 20a for illustration). In practice, for this situation to occur at fields lower than the breakdown field, pairs of lower E_G material(s) such as NiO, ZnO, Nb_2O_5, Ta_2O_5, Co_3O_4, TiO_2, etc. must typically be used.

A third way of engineering asymmetry with the tunnel barrier is enabled by pairing up a narrow E_G insulator dominated by thermal emission-based charge transport with a wide E_G insulator dominated by tunneling. Referred to as defect enhanced direct tunneling (DEDT), this situation is illustrated in Figs. 20b and 20f.[515] In this case, electron transport through the narrow gap insulator is facilitated by defects, such as in Frenkel-Poole emission (FPE), before direct tunneling (DT) through the wider bandgap insulator. This transport occurs at a much higher probability than direct tunneling through the entire thickness of both insulators. As seen in Figs. 20d and 20f the direction of DEDT asymmetry is opposite that of step tunneling. Because the onset of DEDT for this insulator stack occurs at fields below that required for the onset of step tunneling, (i) DEDT will initially dominate over step tunneling and (ii) asymmetry can be engineered to occur at a lower turn on voltage as seen in Fig. 20e. (Note that the RT (illustrated in Fig. 20a) does not play a role as the fields required to reach this situation are well above the breakdown strength of the insulators.)

As with step tunneling, the asymmetry induced by the asymmetric tunnel barrier should align with the asymmetry induced by electrode $\Delta\Phi_M$. When the insulators are deposited in reverse order, DEDT overwhelms the asymmetry induced by $\Delta\Phi_M$ and asymmetry is in the opposite direction (and of lower magnitude).[515] Finally, despite the enhancement of asymmetry by defect emission based transport, because operation under both polarities is limited by direct tunneling, overall device operation is relatively insensitive to temperature.[515]

Interest in thin film multi-insulator MIIM diodes has been increasing and there has been much recent work on thin film MIIM devices using various combinations of insulators and metals, including experimental[510,513,515,516,521,527,533,603–605,609–612] and theory.[613–615] There are also a few reports of multi-insulator MI^3M and MI^4M diodes.[514,608,615,616] Despite the increased interest and great promise of this approach, much work still remains to optimize MIM and MIIM diodes based on employing various metal and insulator combinations as well as processing.

Resistive Switching Random Access Memory (ReRAM)

Another interesting application for high-*k* dielectrics is as a solid-state electrolyte. Electrolyte materials are those that possess an ionic conductivity many orders of magnitude higher than their electronic conductivity.[617] Electrolyte devices, such as batteries, typically utilize liquids as the electrolyte due to their high ionic mobility. However, it turns out that solids such as HfO_2, ZrO_2, TaO_x and other refractory and rare-earth metal oxides exhibit sufficiently fast ionic transport for metal cations (Cu^+, Ag^+, Ni^{2+}) and oxygen vacancy anion defects (V_O^-) to function as solid-state electrolyte materials at dimensions

commonly utilized in state-of-the-art CMOS devices.[618] Numerous books and review articles have been published in the past on solid state ionics.[619] However, thin film electrolyte materials have recently emerged as the heart of a novel non-volatile form of memory (NVM) referred to as resistive RAM (ReRAM). As it turns out, ReRAM is now considered one of the prime candidates to replace the floating gate transistor as the standard NVM memory cell.[620]

A ReRAM device is generally built as a capacitor-like MIM structure comprised of an insulating or resistive material sandwiched between two electronic conductors, such as the Cu/TaO_x/(W or Pt). The Cu electrode, called the active electrode, produces via a redox reaction ($Cu \rightarrow Cu^{+}+e^{-}$) highly mobile Cu^{+} cations that drift in an electric field through TaO_x and discharge at the inert W(Pt) electrode forming backwards a conductive filament (CF) between the two electrodes. Such ReRAM devices are also sometimes referred to as conducting bridging RAM or CBRAM.

Another type of ReRAM memory cell is based on valence or phase change dielectric materials.[620] A well-known example of it is a Pt/TiO_2/Pt cell[621] that has no active electrode just two inert ones (Platinum). Under an electric field, an oxygen ion will be dislodged leaving an oxygen vacancy behind forming a substochiometric oxide TiO_x with $x < 2$. While TiO_2 is insulating, the oxygen-deficient TiO_x phase is highly conductive. Thus, in case of phase change, no conductive filament is being formed, instead the insulating TiO_2 layer changes in bulk to a conductive phase to create electric conduction in the dielectric.[621] The study of phase changing oxides and suboxides is a new exciting area with potential applications not only in memory storage but also in neuromorphic computing.[622,623]

Neuromorphic computing has widely been studied but still on conventional von Neuman architectures and CMOS platforms. The ultimate goal, however, is to perform neuromorphic computing on intrinsically neuromorphic hardware which is anticipated to be less energy consuming, much more computing efficient and much less area intensive. Such revolutionary hardware may be enabled by the memristive properties of the ReRAM devices. As early as in 1971, Professor Chua predicted the existence of a memristor based on circuit theory.[624] Forty years later in 2008, the physical realization of memristor was demonstrated through a TiO_2 thin-film[625] described above in terms of material properties.[621] A memristor is basically a resistor with memory. A memristor exhibits a set of unique fingerprints[626–628] among them a current-voltage pinched hysteretic loop under bipolar excitation. However, such current-voltage characteristics do not uniquely define a memristor. It is the charge-flux (q-φ) relation which does it. The memristor records its total magnetic flux φ as memristance M which describes the charge-dependent rate of change of flux with charge, i.e. $M = d\varphi/dq$. Presently, little is known about how the magnetic flux is stored in dielectric materials and the pertinent field is still in its infancy. Needless to say, the memristor property is highly similar to the weighting function of a biological synapse.

As mentioned above, the two-terminal thin-film device MIM structure can be easily integrated into crossbar arrays. It can provide a large number of signal connections within a small footprint and conduct the weighted combination of input signals, making it very promising for massively-parallel, large-scale neuromorphic systems.[629] Neuromorphic hardware systems inspired by the working mechanism of human brains[630] can potentially provide the capabilities of biological perception and cognitive information processing within a compact and energy-efficient platform. Therefore, the development of neuromorphic circuits has gained a lot of attention in recent years. Examples of some of the neuromorphic functions based on simple two MIM (memristor) configurations have been described in Refs. 631,632.

Low-*k* ReRAM

As with high-*k* dielectrics, numerous new device applications are also emerging for traditional low-*k* dielectrics. In some cases, low- and high-*k* dielectrics are of interest for the same applications. One specific example is as a solid-state electrolyte in ReRAM devices. As previously discussed, solid electrolytes are materials with an ionic conductivity several orders of magnitude higher than their electronic conductivity. In this case, the reliability issues associated with the high mobility of metallic species in low-*k* ILDs[633,634] represents a potential advantage for use of low-*k* materials as solid electrolytes in ReRAM device applications. As an example, a typical Arrhenius diffusion coefficient for Cu in a non-porous low-*k* SiOCH is $\sim 6.1 \times 10^{-9} e^{-0.71\ eV/kT}$ cm^2/s which can displace a Cu atom or ion during backend processing at 400°C a distance of over 20 nm in 5 min.[635] While this diffusional transport poses a serious challenge for metal interconnect reliability, it may lead to new applications in non-volatile memory. Specifically, use of low-*k* dielectrics as a solid-state electrolyte for Cu may allow ReRAM memory cells to be natively embedded in CMOS low-*k*/Cu interconnect structures.

The integration of a ReRAM memory cell directly into a CMOS low-*k*/Cu interconnect would be particularly advantageous as it could help reduce latency in connectivity constrained computational devices and reduce a chip's footprint by stacking memory directly on top of logic. As described above, current interconnect RC scaling methods have reached their limits leaving only a few alternative ways to reduce or remove latency constraints in metal interconnects. In this context, the ReRAM cell appears highly suitable for co-integration and fabrication using exclusively native materials to a standard BEOL interconnect. Further, with continuous dimensional down-scaling, the line-line spacing in advanced metal interconnect structures have now approached 30 nm or less. At these dimensions, the thickness of the electrically insulating low-*k* dielectric isolating the metal lines is so thin that it can potentially function as a solid-state electrolyte for metals (such as Cu) in a similar fashion to that previously discussed above for high-*k* dielectrics. This is in part due to the high diffusion coefficient exhibited by low-*k* ILD dielectrics for metals such as Cu, Ni, and Ag.[633,634]

The current challenge to integrate ReRAM type memory into the CMOS backend consists of achieving material and process compatibility with the current technology. Initial studies have shown that MIM structures such as Cu/SiCOH/W display resistive switching behavior. A recent study[43] has found that currently employed backend porous SiCOH low-*k* dielectrics are compatible with ReRAM functionality. It has been shown that in devices with Cu and W electrodes and porous SiCOH with 8% to 25% porosity resistive switching is feasible. The critical threshold voltages for SET and RESET operations are in the 1 V range: $V_{set} = 0.5V–2.0V$ and $V_{reset} = (-0.8V) - (-1.4V)$. In terms of interconnect reliability, it has been found that higher porosity level shifts the dielectric breakdown voltage to higher values providing thus a wider reliability margin. However, there is trade-off with reliability related to Cu diffusion and to Cu drift transport. As mentioned before, at high porosity levels (30% and higher) interconnected pores are being formed. Interconnected pores offer new efficient Cu transport paths along the pore surfaces. The Cu transport enhancement or retardation depends then on the specific morphology of the pores relative to the direction of the electric field.[188]

Recently, ReRAM type memory operation has also been demonstrated using denser amorphous a-SiOC:H materials typically used as a Cu capping or etch stop layers in low-*k*/Cu interconnects. Use of these materials as the solid-state electrolyte in a ReRAM would be particularly advantageous as they are already directly in contact with Cu in the BEOL. MIM structures for ReRAM could be potentially built into these BEOL interconnects. Figure 21 shows results from a typical a-$SiO_{1.5}C_{0.2}$:H material and the corresponding ReRAM with a-$SiO_{1.5}C_{0.2}$:H as the low-*k* dielectric device layer. The 20 nm thick a-$SiO_{1.5}C_{0.2}$:H film was deposited on a Cu/Ta/TaN/SiN/SiO_2/Si substrate, using a standard BEOL Plasma enhanced chemical vapor deposition (PECVD) process.[218] Subsequently, W electrodes were formed on top of the a-$SiO_{1.5}C_{0.2}$:H layer to form Cu/a-$SiO_{1.5}C_{0.2}$:H/W ReRAM devices, whereby Cu is the active electrode and W is the inert electrode. The a-$SiO_{1.5}C_{0.2}$:H layer has a dielectric constant of 4.3 and a density of 2.4 g/cm^3[218] higher values than that of previously reported a-SiOC:H with density of 1.2 g/cm^3, and contain interconnected pores.[43] Figures 21a and 21b show the ellipsometry results of the refractive index and the bandgap of the a-$SiO_{1.5}C_{0.2}$:H

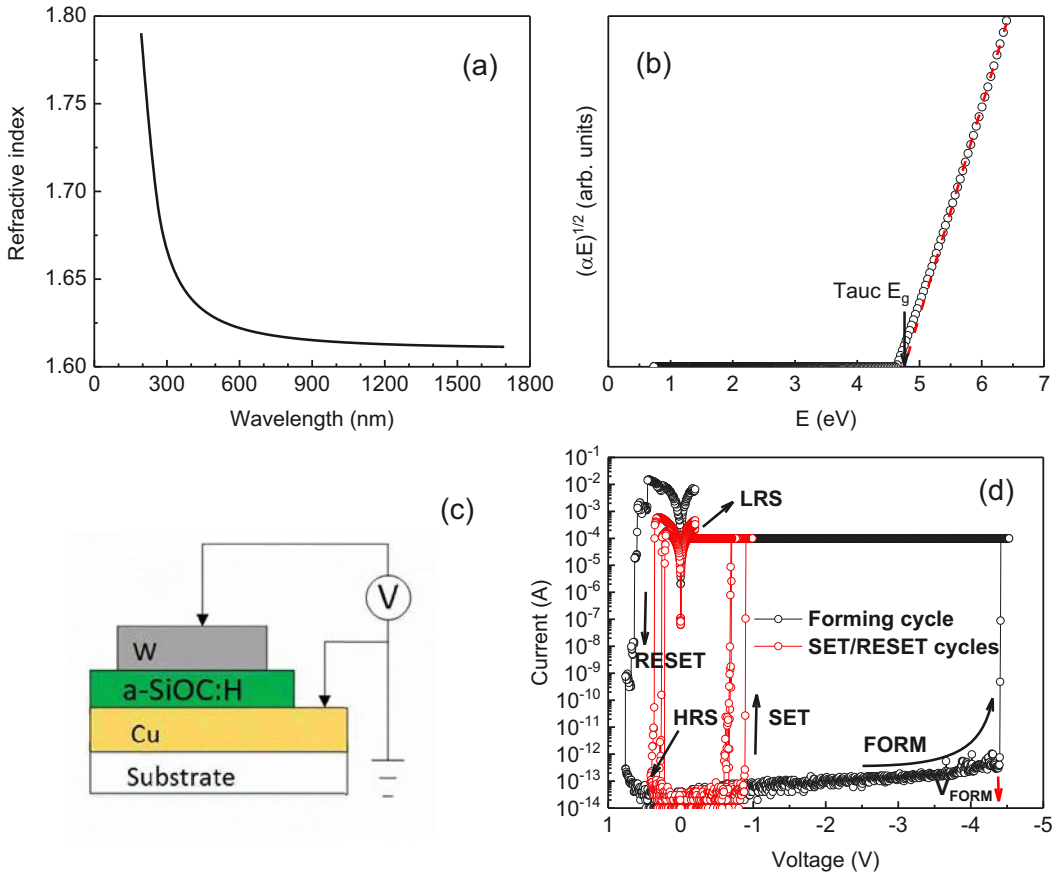

Figure 21. (a) Refractive index of a-$SiO_{1.5}C_{0.2}$:H as a function of wavelength; (b) Tauc plot and bandgap estimation for a-$SiO_{1.5}C_{0.2}$:H; (c) cross-section schematic and measurement setup of the Cu/a-$SiO_{1.5}C_{0.2}$:H/W ReRAM devices; (d) typical I-V characteristics of a device with 40 μm × 40 μm in area, showing the forming switching cycle for the pristine device and the subsequent Set/Rest cycles. The low (LRS) and high (HRS) resistance states are also indicated, while the ON/OFF ratio is defined by the current at LRS over that of HRS.[635]

with values of approximately 1.6 at 673 nm wavelength and 4.8 eV, respectively.

Figure 21c shows a schematic of the device stack and the electrical measurement set up. Figure 21d shows the cycling of the memory showing a forming voltage (V_{FORM}) of approximately 4.3 V. This is higher than that of the counterpart devices using low density a-SiOC:H layers.[43] This is likely because the interconnected pores in low density a-SiOC:H materials which demand lower diffusion energy for Cu ions when subject to electric field. However, in the subsequent SET/RESET switching cycles, ultra-high ON/OFF resistive switching ratios in the order of 10^9–10^{10} were obtained (Figure 21d), over 7 orders of magnitude higher than those from the porous devices.[43] Such ON/OFF ratios are advantageous for future ReRAM applications which can be potentially exploited to implement multilevel storage and also lead to simplified periphery read-out circuits. Recent retention studies in these devices[635] also demonstrated the potential of excellent stability of these devices. Thus, for future BEOL built-in ReRAM devices, trade-off between material properties and ReRAM performance may be needed when selecting the appropriate low-k SiOCH to act as the solid-state electrolyte layers.

As shown in Table VI, both unipolar and bipolar resistive switching/ReRAM functionality has also been demonstrated using as the solid-state electrolyte a host of other silicon-based dielectrics commonly utilized in metal interconnect fabrication including SiO_2, SiO_x, SiN_x, SiC, a-Si:H, and a-C:H.[635–675] Further, the devices demonstrated have also utilized metals native to CMOS processing (Cu, W, Ni, Ta, Ti) and have exhibited low switching voltages, high R_{on}/Ro_{ff} ratios, and impressive endurance and retention performance.[635–675]

Beyond natively embedded ReRAM devices in metal interconnect structures, low-*k* SiOCH materials are also found in a variety of additional device applications ranging from sensors to optoelectronic devices. As described by Jousseaume,[54] the extreme moisture sensitivity of dielectric permittivity for low-*k* SiOCH materials makes them ideal for moisture sensing in MEMS/NEMS packaging.[676] In addition, the porosity and vapor sorption capability that can be achieved with low-*k* SiOCH materials makes these materials attractive as chemically sensitive layers in NEMS based gravimetric gas sensors and miniaturized gas chromatography.[54] In particular, recent results by Boutamine,[677] El Sabahy,[678] and Ricoul[679] have shown that thin film nano-porous SiOCH materials are good candidates for detecting volatile BTEX (benzene, toluene, ethylbenzene, and xylene) air pollutants. The pore size distribution tunability for porous low-*k* SiOCH materials has also recently been utilized for the selective harvesting and detection of small molecules in liquids,[680,681] the extraction of aromatic compounds from water for on chip laboratory analysis,[682] and even reverse osmosis desalination.[683] Porous SiOCH materials are even finding applications as the host material for halogen ion fluorescent optical sensors.[684–686]

Many new applications are also emerging for the non-porous/dense SiOCH and SiCNH materials commonly utilized as etch stop, metal diffusion barriers, and hard masks due to the many other attractive properties they exhibit. As one example, the obsevations of visible-white light luminescence in amorphous SiOCH[687,688] and SiCHN[689–691] thin films has led to their consideration in numerous silicon photonic applications ranging from flat-panel displays to tele-communications.[692–694] The strong resistance of dense SiOCH and SiCNH materials to metal diffusion has also made them of interest as moisture and oxygen permeation/diffusion barriers in pharmaceutical and food packaging[695–698] and organic light emitting diode applications.[699–701] The strong electrochemical stability

of dense SiOC and SiCN materials has even led them to be considered as an anode material in lithium ion batteries and other energy storage applications.[702,703] Finally, the high hardness and chemical inertness of dense SiCNH materials has led to significant interest in these materials for various wear resistant and biocompatible coatings.[704–707]

Dielectric Challenges and Quantum Computing

Aside from directly enabling new beyond CMOS devices and forms of computing, dielectric materials also present in some cases serious roadblocks to these achievements beyond typical electrical, thermal, and mechanical reliability considerations. One specific example concerns the development of various superconducting quantum computing integrated circuits which are viewed as a potential candidate for extending the roadmap for high performance computing by another decade or more.[708,709] Such quantum computers rely on the creation and quantum entanglement of artifical quantum bits ("qubits") from microscopic superconducting device circuits.[710,711] However, the performance of these devices has been shown to be greatly limited by spurious coupling to microscopic defect states present in the amorphous dielectric materials utilized to construct and operate the devices and circuits. This coupling leads to dissipation and dephasing in the superconducting circuit that limits the coherence lifetime of the qubit state.[710] The offending defects are generally attributed to microscopic two-level states (TLS) present in the amorphous materials utilized to implement the qubit circuit.[711] In the tunneling model originally presented by Phillips,[712,713] TLS defects are attributed to atomic scale defects in a potential energy landscape with two local minima separated by a small energy difference that the defect can switch between via either thermal activation or quantum mechanical tunneling.[710] The hopping between the two different states is believed to contribute to the dissipation and loss of coherence lifetimes for qubit states.[711]

Unfortunately, the exact origin, chemical identity, and atomic structure of TLS defects in amorphous materials is not well known despite significant effort in some cases. The origin of TLS defects in amorphous materials have been attributed to everything from "floppy" modes[714–717] or voids[718] in the amorphous structure, hydrogen[58–61,719,720] or moisture (OH) impurities,[721,722] interfacial defects,[723–725] delocalized oxygen atoms,[726–728] surface spin/defects,[57,729,730] and adsorbed oxygen (O_2) molecules.[731–733] It is likely that all these defects in amorphous materials contribute at some level to TLS qubit decoherence. However, significantly more research is needed to identify the dominant ones for specific amorphous materials utilized in qubit manufacture, and, perhaps more importantly, understand the role that material processing and fabrication can play in creating and minimizing TLS defects in amorphous dielectric materials.[62,734]

Toward this end, progress in the field of superconducting computing has been mostly gained by empirically identifying those materials that exhibit low TLS defects/loss[62,701,735–746] and implementing various strategies to minimize the formation of or eliminate the presence of particularly lossy amorphous dielectric materials.[747–753] Toward this end, materials such as c-Si,[735] a-Si:H,[736–738] SiN,[701,739] TiN,[62,740,741] and Nb[742,743] have been identified. However, more low loss materials will likely need to be identified to reach the ultimate goals of high-density qubit integration. As for methods to minimize or eliminate the presence of lossy amorphous dielectrics from qubit circuits, a number of different strategies have been identified including: formation of air-bridge or suspended qubit structures,[747,748] deep trench isolation,[749] epitaxial growth of interfaces,[750–753] minimizing process induced etch damage,[754] improved surface cleaning and preparation,[63,755,756] optimizing thermal processing,[755–759] systematically removing process variation,[760] and continuously improving device construction, geometry, and layout.[761,762] Hereto, additional methods will likely be needed to remove or eliminate TLS defects and lossy dielectrics in order to achieve high density qubit integration. As such, quantum computing represents another fruitful research vector for dielectrics research.

The Other M's: Metrology and Modeling

While this article has focused on how amorphous dielectric materials can enable and support the roadmap for various nanoelectric devices and technologies, it is important to note the significance of the other "m's" needed to reach these achievements.[763] Specifically, substantial advancements in material property and dimensional metrology[764–766] and computational modeling[767–769] will be needed to facilitate the discovery and development of the new materials and process technologies needed to realize the aforementioned roadmaps.[763] For dielectric materials, new metrologies capable of probing atomic structure and thermal and mechanical properties at the nano-scale will be needed.[197,770–775] In this regard, scanning probe/atomic force microscopy (AFM) based techniques such as AFM infrared spectroscopy,[776–780] contact resonance AFM (CR-AFM),[780–788] scanning thermal microscopy[789–794] and related techniques have shown promise for meeting future needs, but still need further research and development to enable routine nanoscale structure-property characterization of dielectric materials.

Techniques capable of identifying and probing individual atomic scale defects and the interfacial structure of dielectrics in actual devices will also be needed. This is particularly the case for the previously mentioned superconducting quantum computing devices which are infinitely more sensitive to low energy TLS defects relative to their CMOS counterparts.[710,711] Here, electrically detected magnetic resonance (EDMR) is one technique that has recently shown the ability to quantitatively detect[795] and identify the structure of defects[796–798] in simple MIM devices and CMOS transistors[796–800] with wafer level probing capability.[801] Related Josephson junction defect spectrometers have also recently been developed for directly probing TLS defects in superconducting qubit devices.[802,803]

It also important to note that the insulating nature of dielectric materials can present additional challenges to more established charge-based techniques such as the scanning and transmission electron microscopies (SEM/TEM) most commonly utilized for imaging and dimensional metrology (film thickness, device critical dimensions).[804] Specifically, the interaction between an electron beam and an insulating material can produce charging and film shrinkage side effects that lead to dubious or erroneous results.[805–808] In this regard, optical and x-ray-based techniques may eliminate some of these issues.[809,810] However, additional non-charge transport-based imaging techniques such as neutral atom microscopy[811,812] and dynamic tunneling force microscopy[813–816] deserve increased attention and represent a potentially fertile area for dielectrics-based metrology research.

Lastly, it is important to emphasize the underlying role that computational modeling has and will continue to play in all facets of the topics covered in this article. During the early searches for possible high-k dielectrics to replace SiO_2 in CMOS devices, theoretical calculations of the high-k/Si substrate valence and conduction band alignments were invaluable in guiding the selection of specific materials for experimental investigation.[2,3] Similarly, computational modeling had a profound impact on the development of low-k materials via providing insight into both structure-property relationships[817–820] and process induced performance and reliability issues.[821–823] The optimal use of high-k and low-k dielectrics in both CMOS transistors, Cu interconnects, and pitch-division patterning stacks was also guided by intensive computational device,[824] thermal-mechanical packaging reliability,[122,123,162–164] and optical proximity correction (OPC) modeling.[147,243,825] Further, computational modeling has already played a significant role in guiding the selection of materials for future beyond CMOS devices and their optimization.[165,170,171,414,826–828] The intensive efforts to identify the chemical origin and structure of TLS defects in superconducting qubit devices described previously is just one example.[726–728] Thus, it can be concluded that computational modeling of materials, devices, and processes will continue to play a substantial role in dielectrics research.

Conclusions

The science of dielectrics has a long history dating back over a century,[8,29] and the past two decades has brought a dizzying array of new materials spanning both the high and low extremes of dielectric permittivity. While further dielectric permittivity scaling may have slowed or reached physical limits, the numerous materials developed and brought forward during this era have created numerous new applications for dielectric materials in both traditional roles as passive electrical isolation and in more diverse roles in enabling new methods of lithographic pattern transfer and in electronic, photonic, and electromechanical devices. Continuing Moore's Law and More than Moore device scaling[93] will require sustained development and refinement of new and existing dielectric materials. Further, new forms of computing such as quantum and neuromorphic will also demand numerous advancements in the field of dielectric science if they are to reach their full potential. In summary, we conclude that the field of dielectrics remains vibrant with numerous exciting new and old research vectors still awaiting further exploration.

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